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May 2012

MM74HC86
Quad 2-Input Exclusive OR Gate

Features

- Typical Propagation Delay: 9ns
- Wide Operating Voltage Range: 2–6V
- Low Input Current: 1mA Maximum
- Low Quiescent Current: 20mA Max. (74 Series)
- Output Drive Capability: 10 LS-TTL Loads

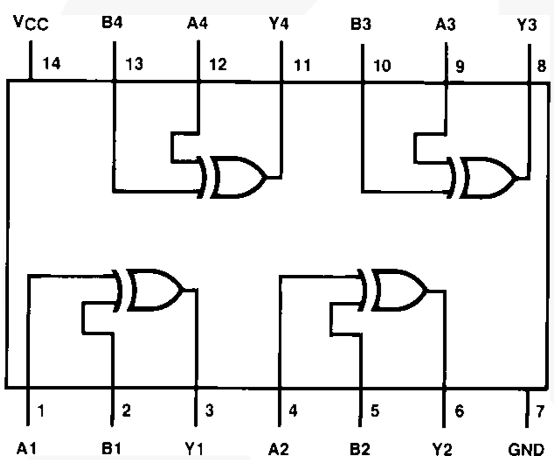


Figure 1. Pin Assignments (Top View)

Description

The MM74HC86 exclusive OR gate utilizes advanced silicon-gate CMOS technology to achieve operating speeds similar to equivalent LS-TTL gates, while maintaining the low power consumption and high noise immunity characteristic of standard CMOS integrated circuits. These gates are fully buffered and have a fanout of 10 LS-TTL loads. The 74HC logic family is functionally as well as pin-out compatible with the standard 74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Table 1. Truth Table

Inputs		Outputs
A	**B**	**Y**(1)
L	L	L
L	H	H
H	L	H
H	H	L

Note:
1. $Y = A \oplus B = \overline{A}B + A\overline{B}$

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
MM74HC86M	-40 to +85°C	14-Lead, Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow	Tube
MM74HC86MX			Tape & Reel
MM74HC86MTC		14-Lead, Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide	Tube
MM74HC86MTCX			Tape & Reel

Note:
2. Pb-Free package per JEDEC J-STD-020B.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. Absolute maximum ratings are stress ratings only. Unless otherwise specified, all voltages are referenced to ground.

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	-0.5	7.0	V
V_{IN}	DC Input Voltage	-1.5	V_{CC} +1.5	V
V_{OUT}	DC Output Voltage	-0.5	V_{CC} +0.5	V
I_{IK}, I_{OK}	Clamp Diode Current	±20		mA
I_{OUT}	DC Output Current, per Pin	±25		mA
I_{CC}	DC VCC or GND Current, per Pin	±50		mA
T_{STG}	Storage Temperature Range	-65	+150	°C
T_L	Lead Temperature (Soldering, 10 Seconds)		260	°C
P_D	Power Dissipation[3, 4]		600	mW

Note:

3. Power dissipation temperature derating — plastic "N" package: -12 mW/°C from 65°C to 85°C.
4. S.O. package only 500mW.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{CC}	Supply Voltage		2	6	V
V_{IN}, V_{OUT}	DC Input or Output Voltage		0	V_{CC}	V
T_A	Operating Temperature Range		-40	+85	°C
t_R, t_F	Input Rise or Fall Times	V_{CC} = 2.0V		1000	ns
		V_{CC} = 4.5V		500	
		V_{CC} = 6.0V		400	

DC Electrical Characteristics[5]

Symbol	Parameter	Condition	V_{CC} (V)	T_A=25°C		T_A=-40 to +85°C	T_A=-55 to +125°C	Units
				Typ.	Guaranteed Limit			
V_{IH}	Minimum HIGH Level Input Voltage		2.0		1.5	1.5	1.5	V
			4.5		3.15	3.15	3.15	
			6.0		4.2	4.2	4.2	
V_{IL}	Maximum LOW Level Input Voltage		2.0		0.5	0.5	0.5	V
			4.5		1.35	1.35	1.35	
			6.0		1.8	1.8	1.8	
V_{OH}	Minimum HIGH Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL}, $\|I_{OUT}\| \leq 20\mu A$	2.0	2.0	1.9	1.9	1.9	V
			4.5	4.5	4.4	4.4	4.4	
			6.0	6.0	5.9	5.9	5.9	
		$V_{IN} = V_{IH}$ or V_{IL}, $\|I_{OUT}\| \leq 4.0mA$	4.5	4.2	3.98	3.84	3.70	
		$V_{IN} = V_{IH}$ or V_{IL}, $\|I_{OUT}\| \leq 5.2mA$	6.0	5.7	5.48	5.34	5.20	
V_{OL}	Maximum LOW Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL}, $\|I_{OUT}\| \leq 20\mu A$	2.0	0	0.1	0.1	0.1	V
			4.5	0	0.1	0.1	0.1	
			6.0	0	0.1	0.1	0.1	
		$V_{IN} = V_{IH}$ or V_{IL}, $\|I_{OUT}\| \leq 4.0mA$	4.5	0.2	0.26	0.33	0.40	
		$V_{IN} = V_{IH}$ or V_{IL}, $\|I_{OUT}\| \leq 5.2mA$	6.0	0.2	0.26	0.33	0.40	
I_{IN}	Maximum Input Current	$V_{IN} = V_{CC}$ or GND	6.0		±0.1	±1.0	±1.0	mA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND, I_{OUT} = 0mA	6.0		2.0	20	40	mA

Note:

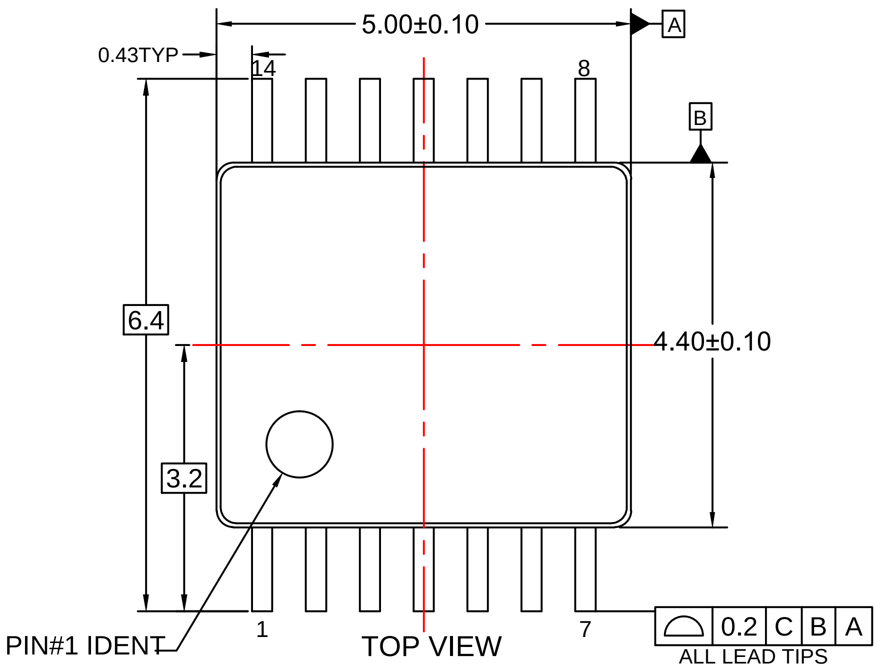
5. For a power supply of 5V ±10%, the worst-case output voltages (V_{OH} and V_{OL}) occur for HC at 4.5V. Thus, the 4.5V values should be used when designing with this supply. Worst-case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V, respectively. (The V_{IH} values at 5V and 5.5V are 3.5V and 3.85V, respectively.) The worst-case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occurs for CMOS at the higher voltage, so the 6.0V values should be used.

AC Electrical Characteristics

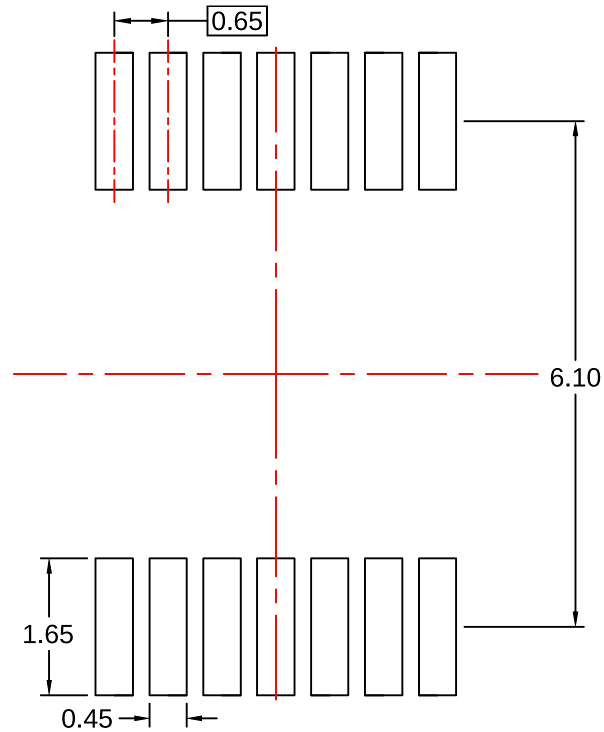
Symbol	Parameter	Conditions	V_{CC}	T_A=25°C		T_A=-40 to +85°C	T_A=-55 to +125°C	Units
				Typ.	Guaranteed Limit			
t_{PHL}, t_{PLH}	Maximum Propagation Delay	C_L = 15pF, $t_R = t_F$ = 6ns	5.0	12		20		ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay	C_L = 50pF, $t_R = t_F$ = 6ns	2.0	60	120	151	179	ns
			4.5	12	24	30	36	
			6.0	10	20	26	30	
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0	30	75	95	110	ns
			4.5	8	15	19	22	
			6.0	7	13	16	19	
C_{PD}	Power Dissipation Capacitance (per Gate)[6]			25				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note:

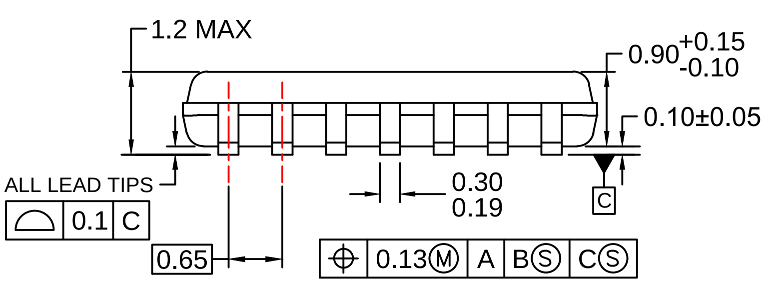
6. C_{PD} determines the no-load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.



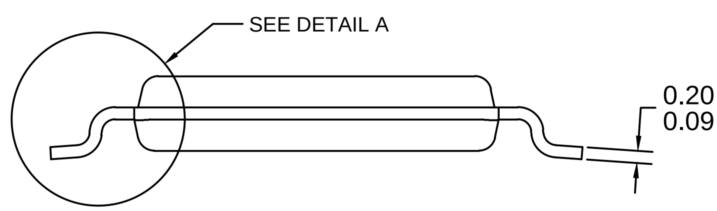
TOP VIEW

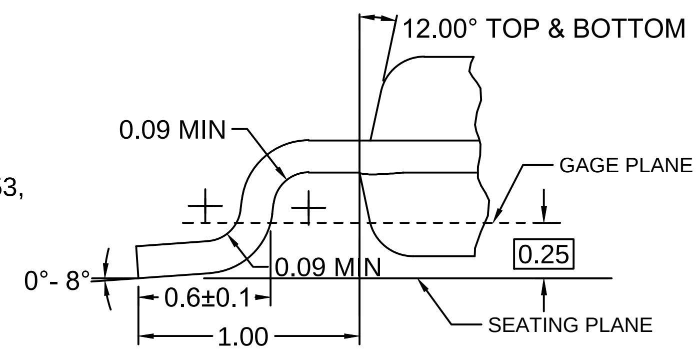


RECOMMENDED LAND PATTERN



FRONT VIEW

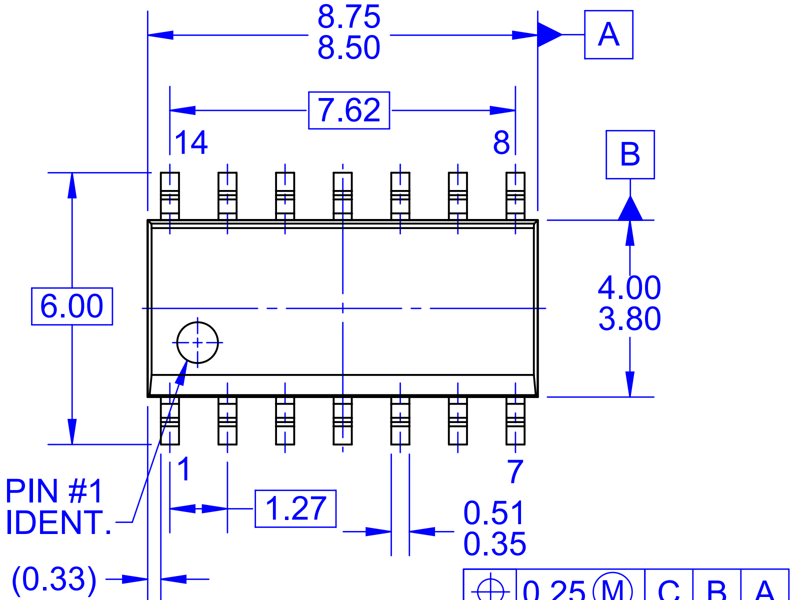




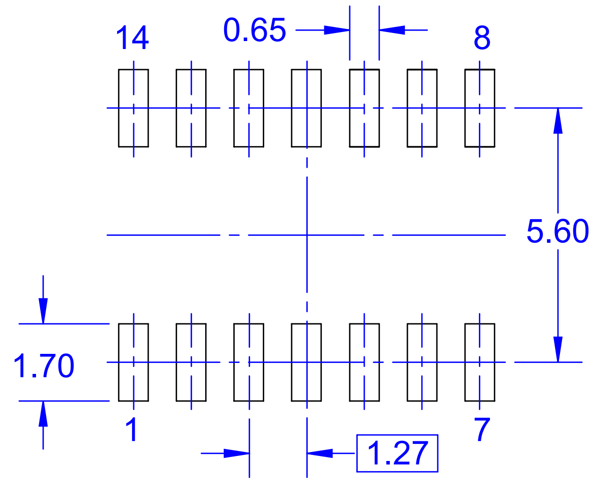
DETAIL A

NOTES:

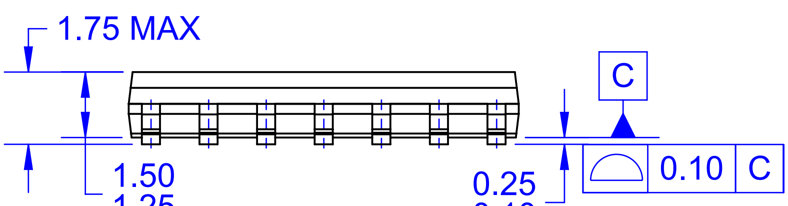
A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 2009.
E. LANDPATTERN STANDARD: SOP65P640X110-14M.
F. DRAWING FILE NAME: MKT-MTC14rev7.



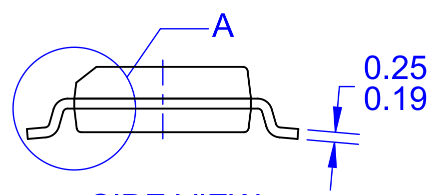
TOP VIEW



LAND PATTERN RECOMMENDATION



FRONT VIEW



SIDE VIEW

NOTES:

A. CONFORMS TO JEDEC MS-012, VARIATION AB, ISSUE C

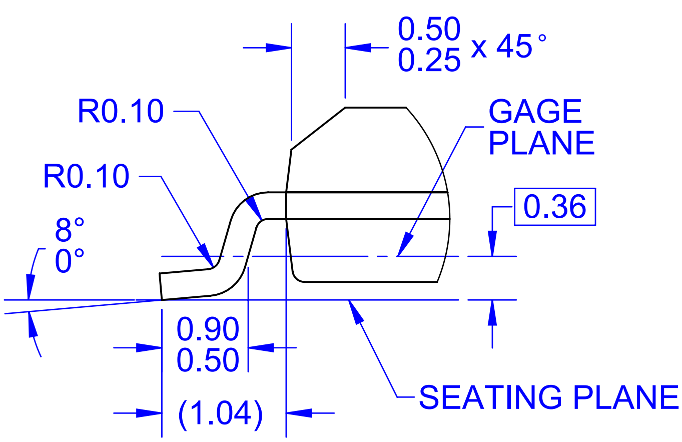
B. ALL DIMENSIONS ARE IN MILLIMETERS

C. DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS

D. LAND PATTERN STANDARD: SOIC127P600X145-14M

E. CONFORMS TO ASME Y14.5M, 2009

D. DRAWING FILENAME: MKT-M14Arev14



DETAIL A
SCALE 16 : 1

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