



CD4066BM/CD4066BC Quad Bilateral Switch

General Description

The CD4066BM/CD4066BC is a quad bilateral switch intended for the transmission or multiplexing of analog or digital signals. It is pin-for-pin compatible with CD4016BM/CD4016BC, but has a much lower "ON" resistance, and "ON" resistance is relatively constant over the input-signal range.

- Extremely low "OFF" switch leakage @ $V_{DD} - V_{SS} = 10V, T_A = 25^\circ C$ 0.1 nA (typ.)
- Extremely high control input impedance $10^{12}\Omega$ (typ.)
- Low crosstalk between switches @ $f_{is} = 0.9 \text{ MHz}, R_L = 1 \text{ k}\Omega$ - 50 dB (typ.)
- Frequency response, switch "ON" 40 MHz (typ.)

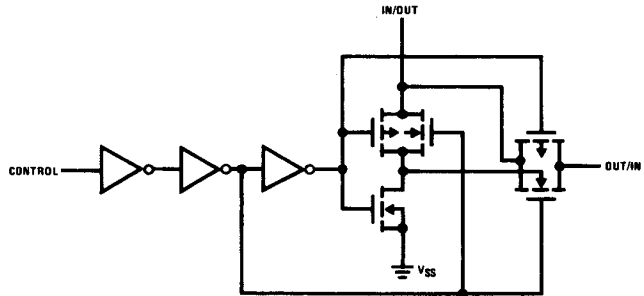
Features

- Wide supply voltage range 3V to 15V
- High noise immunity 0.45 V_{DD} (typ.)
- Wide range of digital and analog switching $\pm 7.5 V_{PEAK}$
- "ON" resistance for 15V operation 80 Ω
- Matched "ON" resistance over 15V signal input $\Delta R_{ON} = 5\Omega$ (typ.)
- "ON" resistance flat over peak-to-peak signal range
- High "ON"/"OFF" output voltage ratio 65 dB (typ.) @ $f_{is} = 10 \text{ kHz}, R_L = 10 \text{ k}\Omega$
- High degree linearity 0.1% distortion (typ.) @ $f_{is} = 1 \text{ kHz}, V_{is} = 5V_{p-p}, V_{DD} - V_{SS} = 10V, R_L = 10 \text{ k}\Omega$
- High degree linearity
- High degree linearity

Applications

- Analog signal switching/multiplexing
 - Signal gating
 - Squelch control
 - Chopper
 - Modulator/Demodulator
 - Commutating switch
- Digital signal switching/multiplexing
- CMOS logic implementation
- Analog-to-digital/digital-to-analog conversion
- Digital control of frequency, impedance, phase, and analog-signal-gain

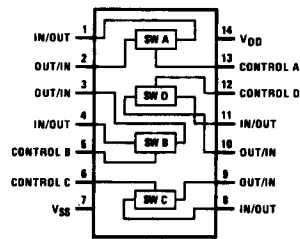
Schematic and Connection Diagrams



Order Number CD4066B*

*Please look into Section 8, Appendix B for availability of various package types.

Dual-In-Line Package



Top View

TL/F/5665-1

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{DD})	-0.5V to +18V
Input Voltage (V_{IN})	-0.5V to $V_{DD} + 0.5V$
Storage Temperature Range (T_S)	-65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L)	
(Soldering, 10 seconds)	300°C

Recommended Operating Conditions (Note 2)

Supply Voltage (V_{DD})	3V to 15V
Input Voltage (V_{IN})	0V to V_{DD}
Operating Temperature Range (T_A)	
CD4066BM	-55°C to +125°C
CD4066BC	-40°C to +85°C

DC Electrical Characteristics CD4066BM (Note 2)

Symbol	Parameter	Conditions	-55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V$		0.25		0.01	0.25		7.5	μA
		$V_{DD} = 10V$		0.5		0.01	0.5		15	μA
		$V_{DD} = 15V$		1.0		0.01	1.0		30	μA

SIGNAL INPUTS AND OUTPUTS

R_{ON}	"ON" Resistance	$R_L = 10\text{ k}\Omega$ to $\frac{V_{DD} - V_{SS}}{2}$ $V_C = V_{DD}$, $V_{IS} = V_{SS}$ to V_{DD} $V_{DD} = 5V$ $V_{DD} = 10V$ $V_{DD} = 15V$		800 310 200		270 120 80	1050 400 240		1300 550 320	Ω Ω Ω
ΔR_{ON}	Δ "ON" Resistance Between any 2 of 4 Switches	$R_L = 10\text{ k}\Omega$ to $\frac{V_{DD} - V_{SS}}{2}$ $V_C = V_{DD}$, $V_{IS} = V_{SS}$ to V_{DD} $V_{DD} = 10V$ $V_{DD} = 15V$				10 5				Ω Ω
I_{IS}	Input or Output Leakage Switch "OFF"	$V_C = 0$ $V_{IS} = 15V$ and $0V$, $V_{OS} = 0V$ and $15V$		± 50		± 0.1	± 50		± 500	nA

CONTROL INPUTS

V_{ILC}	Low Level Input Voltage	$V_{IS} = V_{SS}$ and V_{DD} $V_{OS} = V_{DD}$ and V_{SS} $I_{IS} = \pm 10\ \mu A$ $V_{DD} = 5V$ $V_{DD} = 10V$ $V_{DD} = 15V$		1.5 3.0 4.0		2.25 4.5 6.75	1.5 3.0 4.0		1.5 3.0 4.0	V V V
V_{IHC}	High Level Input Voltage	$V_{DD} = 5V$ $V_{DD} = 10V$ (see note 6) $V_{DD} = 15V$	3.5 7.0 11.0		3.5 7.0 11.0	2.75 5.5 8.25		3.5 7.0 11.0		V V V
I_{IN}	Input Current	$V_{DD} - V_{SS} = 15V$ $V_{DD} \geq V_{IS} \geq V_{SS}$ $V_{DD} \geq V_C \geq V_{SS}$		± 0.1		$\pm 10^{-5}$	± 0.1		± 1.0	μA

DC Electrical Characteristics CD4066BC (Note 2)

Symbol	Parameter	Conditions	-40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V$		1.0		0.01	1.0		7.5	μA
		$V_{DD} = 10V$		2.0		0.01	2.0		15	μA
		$V_{DD} = 15V$		4.0		0.01	4.0		30	μA

DC Electrical Characteristics (Continued) CD4066BC (Note 2)

Symbol	Parameter	Conditions	-40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
SIGNAL INPUTS AND OUTPUTS										
R _{ON}	"ON" Resistance	R _L = 10 kΩ to $\frac{V_{DD}-V_{SS}}{2}$ V _C = V _{DD} , V _{SS} to V _{DD} V _{DD} = 5V V _{DD} = 10V V _{DD} = 15V		850 330 210		270 120 80	1050 400 240		1200 520 300	Ω Ω Ω
ΔR _{ON}	Δ"ON" Resistance Between Any 2 of 4 Switches	R _L = 10 kΩ to $\frac{V_{DD}-V_{SS}}{2}$ V _{CC} = V _{DD} , V _{IS} = V _{SS} to V _{DD} V _{DD} = 10V V _{DD} = 15V				10 5				Ω Ω
I _{IS}	Input or Output Leakage Switch "OFF"	V _C = 0		± 50		± 0.1	± 50		± 200	nA
CONTROL INPUTS										
V _{ILC}	Low Level Input Voltage	V _{IS} = V _{SS} and V _{DD} V _{OS} = V _{DD} and V _{SS} I _{IS} = ± 10 μA V _{DD} = 5V V _{DD} = 10V V _{DD} = 15V		1.5 3.0 4.0		2.25 4.5 6.75	1.5 3.0 4.0		1.5 3.0 4.0	V V V
V _{IHC}	High Level Input Voltage	V _{DD} = 5V V _{DD} = 10V (See note 6) V _{DD} = 15V	3.5 7.0 11.0		3.5 7.0 11.0	2.75 5.5 8.25		3.5 7.0 11.0		V V V
I _{IN}	Input Current	V _{DD} - V _{SS} = 15V V _{DD} ≥ V _{IS} ≥ V _{SS} V _{DD} ≥ V _C ≥ V _{SS}		± 0.3		± 10 ⁻⁵	± 0.3		± 1.0	μA

AC Electrical Characteristics* T_A = 25°C, t_r = t_f = 20 ns and V_{SS} = 0V unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units	
t _{PHL} , t _{PLH}	Propagation Delay Time Signal Input to Signal Output	V _C = V _{DD} , C _L = 50 pF, (Figure 1) R _L = 200k V _{DD} = 5V V _{DD} = 10V V _{DD} = 15V			25 15 10	ns ns ns	
t _{PZH} , t _{PZL}	Propagation Delay Time Control Input to Signal Output High Impedance to Logical Level	R _L = 1.0 kΩ, C _L = 50 pF, (Figures 2 and 3) V _{DD} = 5V V _{DD} = 10V V _{DD} = 15V				125 60 50	ns ns ns
t _{PHZ} , t _{PLZ}	Propagation Delay Time Control Input to Signal Output Logical Level to High Impedance Sine Wave Distortion	R _L = 1.0 kΩ, C _L = 50 pF, (Figures 2 and 3) V _{DD} = 5V V _{DD} = 10V V _{DD} = 15V V _C = V _{DD} = 5V, V _{SS} = -5V R _L = 10 kΩ, V _{IS} = 5V _{p-p} , f = 1 kHz, (Figure 4)			0.1	ns ns ns %	
	Frequency Response-Switch "ON" (Frequency at -3 dB)	V _C = V _{DD} = 5V, V _{SS} = -5V, R _L = 1 kΩ, V _{IS} = 5V _{p-p} , 20 Log ₁₀ V _{OS} /V _{OS} (1 kHz) - dB, (Figure 4)			40	MHz	

AC Electrical Characteristics* (Continued) $T_A = 25^\circ\text{C}$, $t_r = t_f = 20\text{ ns}$ and $V_{SS} = 0\text{V}$ unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Feedthrough — Switch "OFF" (Frequency at -50 dB)	$V_{DD} = 5.0\text{V}$, $V_{CC} = V_{SS} = -5.0\text{V}$, $R_L = 1\text{ k}\Omega$, $V_{IS} = 5.0\text{V}_{p-p}$, 20 Log ₁₀ , $V_{OS}/V_{IS} = -50\text{ dB}$, (Figure 4)		1.25		
	Crosstalk Between Any Two Switches (Frequency at -50 dB)	$V_{DD} = V_{C(A)} = 5.0\text{V}$; $V_{SS} = V_{C(B)} = 5.0\text{V}$, $R_L 1\text{ k}\Omega$, $V_{IS(A)} = 5.0\text{V}_{p-p}$, 20 Log ₁₀ , $V_{OS(B)}/V_{IS(A)} = -50\text{ dB}$ (Figure 5)		0.9		MHz
	Crosstalk; Control Input to Signal Output	$V_{DD} = 10\text{V}$, $R_L = 10\text{ k}\Omega$, $R_{IN} = 1.0\text{ k}\Omega$, $V_{CC} = 10\text{V}$ Square Wave, $C_L = 50\text{ pF}$ (Figure 6)		150		mV _{p-p}
	Maximum Control Input	$R_L = 1.0\text{ k}\Omega$, $C_L = 50\text{ pF}$, (Figure 7) $V_{OS(f)} = 1/2 V_{OS}(1.0\text{ kHz})$ $V_{DD} = 5.0\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		6.0 8.0 8.5		MHz MHz MHz
C_{IS}	Signal Input Capacitance			8.0		pF
C_{OS}	Signal Output Capacitance	$V_{DD} = 10\text{V}$		8.0		pF
C_{IOS}	Feedthrough Capacitance	$V_C = 0\text{V}$		0.5		pF
C_{IN}	Control Input Capacitance			5.0	7.5	pF

*AC Parameters are guaranteed by DC correlated testing.

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: $V_{SS} = 0\text{V}$ unless otherwise specified.

Note 3: These devices should not be connected to circuits with the power "ON".

Note 4: In all cases, there is approximately 5 pF of probe and jig capacitance in the output; however, this capacitance is included in C_L wherever it is specified.

Note 5: V_{IS} is the voltage at the in/out pin and V_{OS} is the voltage at the out/in pin. V_C is the voltage at the control input.

Note 6: Conditions for V_{IHC} : a) $V_{IS} = V_{DD}$, $I_{OS} = \text{standard B series } I_{OH}$ b) $V_{IS} = 0\text{V}$, $I_{OL} = \text{standard B series } I_{OL}$.

AC Test Circuits and Switching Time Waveforms

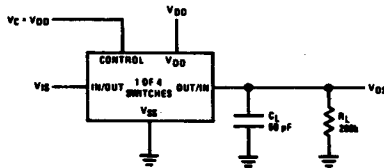


FIGURE 1. t_{PHL} , t_{PLH} Propagation Delay Time Signal Input to Signal Output

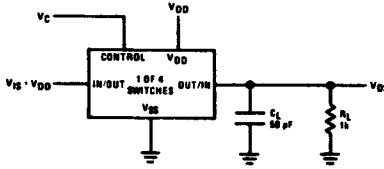
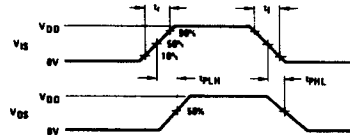


FIGURE 2. t_{PZH} , t_{PHZ} Propagation Delay Time Control to Signal Output

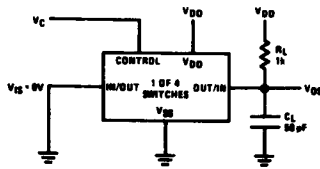
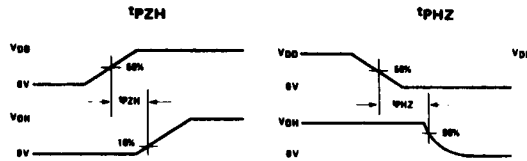
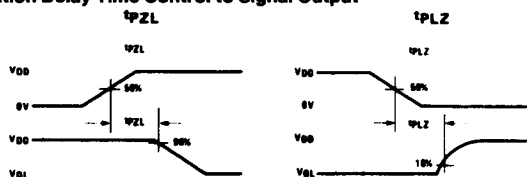
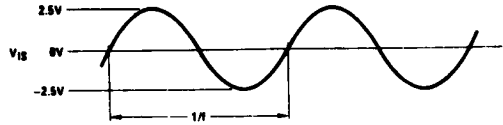
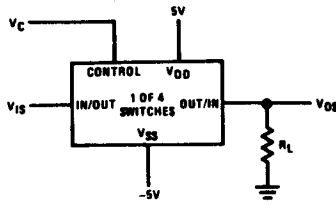


FIGURE 3. t_{PZL} , t_{PLZ} Propagation Delay Time Control to Signal Output



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AC Test Circuits and Switching Time Waveforms (Continued)



$V_C = V_{DD}$ for distortion and frequency response tests
 $V_C = V_{SS}$ for feedthrough test

FIGURE 4. Sine Wave Distortion, Frequency Response and Feedthrough

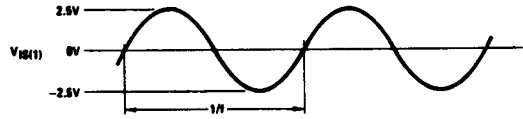
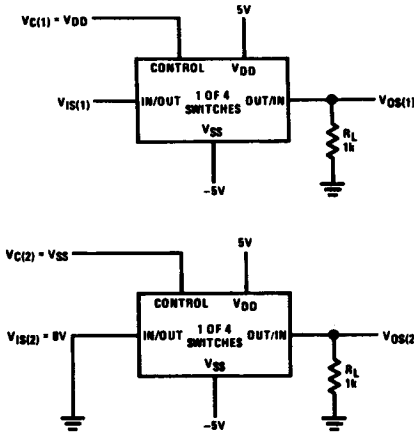


FIGURE 5. Crosstalk Between Any Two Switches

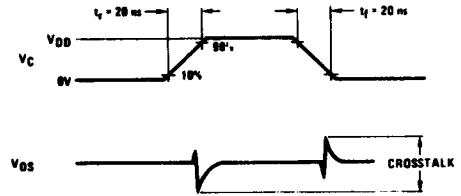
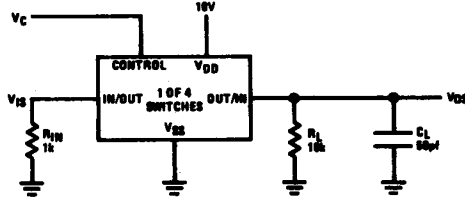


FIGURE 6. Crosstalk: Control Input to Signal Output

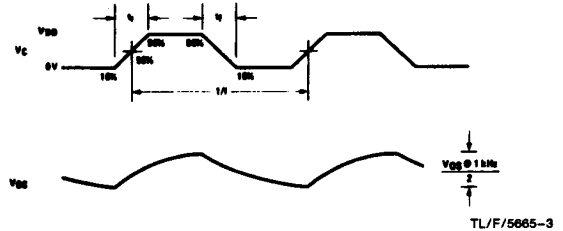
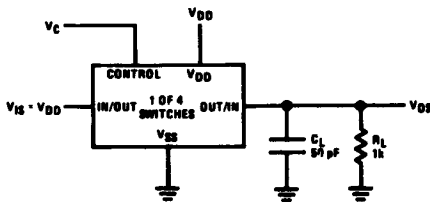
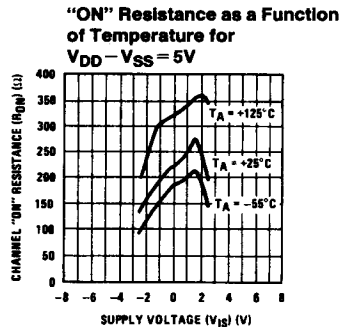
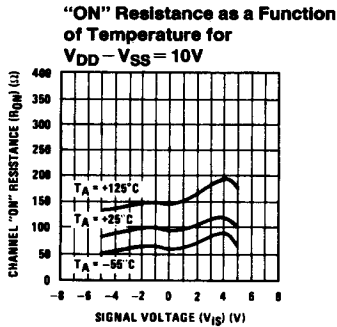
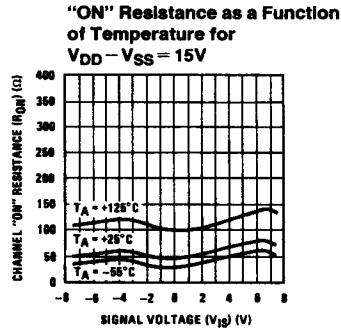
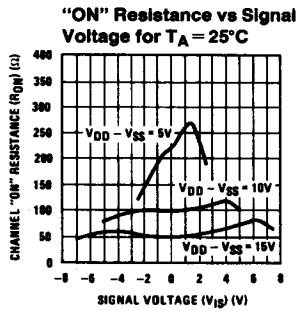


FIGURE 7. Maximum Control Input Frequency

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Typical Performance Characteristics



TL/F/5665-4

Special Considerations

In applications where separate power sources are used to drive V_{DD} and the signal input, the V_{DD} current capability should exceed V_{DD}/R_L (R_L = effective external load of the 4 CD4066BM/CD4066BC bilateral switches). This provision avoids any permanent current flow or clamp action of the V_{DD} supply when power is applied or removed from CD4066BM/CD4066BC.

In certain applications, the external load-resistor current may include both V_{DD} and signal-line components. To avoid

drawing V_{DD} current when switch current flows into terminals 1, 4, 8 or 11, the voltage drop across the bidirectional switch must not exceed 0.6V at $T_A \leq 25^\circ\text{C}$, or 0.4V at $T_A > 25^\circ\text{C}$ (calculated from R_{ON} values shown).

No V_{DD} current will flow through R_L if the switch current flows into terminals 2, 3, 9 or 10.