

**OPA342**  
**OPA2342**  
**OPA4342**

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## Low Cost, Low Power, Rail-to-Rail OPERATIONAL AMPLIFIERS

### *MicroAmplifier™* Series

#### FEATURES

- **LOW QUIESCENT CURRENT:** 150 $\mu$ A typ
- **RAIL-TO-RAIL INPUT**
- **RAIL-TO-RAIL OUTPUT (within 1mV)**
- **SINGLE SUPPLY CAPABILITY**
- **LOW COST**
- **MicroSIZE PACKAGE OPTIONS:**
  - SOT-23-5
  - MSOP-8
  - TSSOP-14<sup>(1)</sup>
- **BANDWIDTH:** 1MHz
- **SLEW RATE:** 1V/ $\mu$ s
- **THD + NOISE:** 0.006%

#### APPLICATIONS

- **COMMUNICATIONS**
- **PCMCIA CARDS**
- **DATA ACQUISITION**
- **PROCESS CONTROL**
- **AUDIO PROCESSING**
- **ACTIVE FILTERS**
- **TEST EQUIPMENT**
- **CONSUMER ELECTRONICS**

#### DESCRIPTION

The OPA342 series rail-to-rail CMOS operational amplifiers are designed for low cost, low power, miniature applications. They are optimized to operate on a single supply as low as 2.5V with an input common-mode voltage range that extends 300mV beyond the supplies.

Rail-to-rail input/output and high-speed operation make them ideal for driving sampling analog-to-digital converters. They are also well suited for general purpose and audio applications and providing I/V conversion at the output of digital-to-analog converters. Single, dual, and quad versions have identical specs for design flexibility.

The OPA342 series offers excellent dynamic response with a quiescent current of only 250 $\mu$ A max. Dual and quad designs feature completely independent circuitry for lowest crosstalk and freedom from interaction.

The OPA342 is available in the microsize SOT-23-5 and SO-8 packages. The OPA2342 is available in the MSOP-8 and SO-8 packages. The OPA4342 is available in TSSOP-14<sup>(1)</sup> and SO-14 packages. All are specified for operation from -40°C to +85°C. A SPICE macromodel is available for design analysis.

NOTE: (1) TSSOP-14 package available Q4'99.

SPICE MODEL available at [www.burr-brown.com](http://www.burr-brown.com).

# SPECIFICATIONS: $V_S = 2.7V$ to $5.5V$

At  $T_A = +25^\circ C$ ,  $R_L = 10k\Omega$  connected to  $V_S/2$  and  $V_{OUT} = V_S/2$ , unless otherwise noted.  
**Boldface** limits apply over the specified temperature range,  $T_A = -40^\circ C$  to  $+85^\circ C$ .

| PARAMETER  | CONDITION  | OPA342NA, UA<br>OPA2342EA, UA<br>OPA4342EA <sup>(1)</sup> , UA |   |   | UNITS  |
|--|--|--|---|---|--|
|  |  | MIN  | TYP   | MAX   |  |
| <b>OFFSET VOLTAGE</b><br>Input Offset Voltage $V_{OS}$<br>$T_A = -40^\circ C$ to $+85^\circ C$<br><b>vs Temperature</b><br>$dV_{OS}/dT$<br>vs Power Supply PSRR<br>$T_A = -40^\circ C$ to $+85^\circ C$<br>Channel Separation, dc<br>$f = 1kHz$  | $V_{CM} = V_S/2$<br><br>$V_S = 2.7V$ to $5.5V$ , $V_{CM} < (V+) - 1.8V$<br>$V_S = 2.7V$ to $5.5V$ , $V_{CM} < (V+) - 1.8V$   |  | $\pm 1$<br>$\pm 1$<br>$\pm 3$<br>30<br><br>0.2<br>132 | $\pm 6$<br>$\pm 6$<br><br>200<br><b>200</b> | mV<br><b>mV</b><br>$\mu V/^\circ C$<br>$\mu V/V$<br>$\mu V/V$<br>$\mu V/V$<br>dB                                       |
| <b>INPUT BIAS CURRENT</b><br>Input Bias Current $I_B$<br>$T_A = -40^\circ C$ to $+85^\circ C$<br>Input Offset Current $I_{OS}$   |  |  | $\pm 0.2$<br>See Typical Curve<br>$\pm 0.2$           | $\pm 10$<br><br>$\pm 10$                    | pA<br><b>pA</b><br>pA  |
| <b>NOISE</b><br>Input Voltage Noise, $f = 0.1Hz$ to $50kHz$<br>Input Voltage Noise Density, $f = 1kHz$ $e_n$<br>Current Noise Density, $f = 1kHz$ $i_n$  |  |  | 8<br>30<br>3  |   | $\mu V_{rms}$<br>$nV/\sqrt{Hz}$<br>$fA/\sqrt{Hz}$  |
| <b>INPUT VOLTAGE RANGE</b><br>Common-Mode Voltage Range $V_{CM}$<br>Common-Mode Rejection Ratio CMRR<br>$T_A = -40^\circ C$ to $+85^\circ C$<br>Common-Mode Rejection Ratio CMRR<br>$T_A = -40^\circ C$ to $+85^\circ C$<br>Common-Mode Rejection Ratio CMRR<br>$T_A = -40^\circ C$ to $+85^\circ C$ | $V_S = +5.5V$ , $-0.3V < V_{CM} < (V+) - 1.8V$<br>$V_S = +5.5V$ , $-0.3V < V_{CM} < (V+) - 1.8V$<br>$V_S = +5.5V$ , $-0.3V < V_{CM} < 5.8V$<br>$V_S = +5.5V$ , $-0.3V < V_{CM} < 5.8V$<br>$V_S = +2.7V$ , $-0.3V < V_{CM} < 3V$<br>$V_S = +2.7V$ , $-0.3V < V_{CM} < 3V$ | -0.3<br>76<br>74<br>66<br>64<br>62<br>60                       | 88<br><br>78<br><br>74                                | (V+) + 0.3<br><br><br><br><br><br>          | V<br>dB<br><b>dB</b><br>dB<br><b>dB</b><br>dB<br><b>dB</b>   |
| <b>INPUT IMPEDANCE</b><br>Differential<br>Common-Mode  |  |  | $10^{13} \parallel 3$<br>$10^{13} \parallel 6$        |   | $\Omega \parallel pF$<br>$\Omega \parallel pF$   |
| <b>OPEN-LOOP GAIN</b><br>Open-Loop Voltage Gain $A_{OL}$<br>$T_A = -40^\circ C$ to $+85^\circ C$<br><br>$T_A = -40^\circ C$ to $+85^\circ C$   | $R_L = 100k\Omega$ , $10mV < V_O < (V+) - 10mV$<br>$R_L = 100k\Omega$ , $10mV < V_O < (V+) - 10mV$<br>$R_L = 5k\Omega$ , $400mV < V_O < (V+) - 400mV$<br>$R_L = 5k\Omega$ , $400mV < V_O < (V+) - 400mV$   | 106<br><b>100</b><br>96<br><b>90</b>                           | 124<br><br>114  |   | dB<br><b>dB</b><br>dB<br><b>dB</b>   |
| <b>FREQUENCY RESPONSE</b><br>Gain-Bandwidth Product GBW<br>Slew Rate SR<br>Settling Time, 0.1%<br>0.01%<br>Overload Recovery Time<br>Total Harmonic Distortion + Noise, $f = 1kHz$ THD+N   | $C_L = 100pF$<br>$G = 1$<br>$G = 1$<br>$V_S = 5.5V$ , 2V Step<br>$V_S = 5.5V$ , 2V Step<br>$V_{IN} \cdot G = V_S$<br>$V_S = 5.5V$ , $V_O = 3Vp-p^{(2)}$ , $G = 1$  |  | 1<br>1<br>5<br>8<br>2.5<br>0.006                      |   | MHz<br>V/ $\mu s$<br>$\mu s$<br>$\mu s$<br>$\mu s$<br>%  |
| <b>OUTPUT</b><br>Voltage Output Swing from Rail <sup>(3)</sup><br><br>$T_A = -40^\circ C$ to $+85^\circ C$<br><br>$T_A = -40^\circ C$ to $+85^\circ C$<br>Short-Circuit Current $I_{SC}$<br>Capacitive Load Drive $C_{LOAD}$   | $R_L = 100k\Omega$ , $A_{OL} \geq 96dB$<br>$R_L = 100k\Omega$ , $A_{OL} \geq 106dB$<br>$R_L = 100k\Omega$ , $A_{OL} \geq 100dB$<br>$R_L = 5k\Omega$ , $A_{OL} \geq 96dB$<br>$R_L = 5k\Omega$ , $A_{OL} \geq 90dB$<br>Per Channel   |  | 1<br>3<br><br>20<br><br>$\pm 15$                      | 10<br><b>10</b><br>400<br><b>400</b>        | mV<br>mV<br><b>mV</b><br>mV<br><b>mV</b><br>mA   |
| <b>POWER SUPPLY</b><br>Specified Voltage Range $V_S$<br>Operating Voltage Range<br>Quiescent Current (per amplifier) $I_Q$<br>$T_A = -40^\circ C$ to $+85^\circ C$   | $I_O = 0A$   | 2.7  | 2.5 to 5.5<br>150                                     | 5.5<br>250<br><b>300</b>                    | V<br>V<br>$\mu A$<br>$\mu A$   |
| <b>TEMPERATURE RANGE</b><br>Specified Range<br>Operating Range<br>Storage Range<br>Thermal Resistance $\theta_{JA}$<br>SOT-23-5 Surface Mount<br>MSOP-8 Surface Mount<br>SO-8 Surface Mount<br>TSSOP-14 Surface Mount <sup>(1)</sup><br>SO-14 Surface Mount  |  | -40<br>-55<br>-65  |   | +85<br>+125<br>+150                         | $^\circ C$<br>$^\circ C$<br>$^\circ C$<br>$^\circ C/W$<br>$^\circ C/W$<br>$^\circ C/W$<br>$^\circ C/W$<br>$^\circ C/W$ |

NOTES: (1) OPA4342EA available 4Q'99. (2)  $V_{OUT} = 0.25V$  to  $3.25V$ . (3) Output voltage swings are measured between the output and power supply rails.

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

|  |                            |
|--|----------------------------|
| Supply Voltage, V+ to V- .....                       | 5.5V                       |
| Signal Input Terminals, Voltage <sup>(2)</sup> ..... | (V-) - 0.5V to (V+) + 0.5V |
| Current <sup>(2)</sup> .....                         | 10mA                       |
| Output Short Circuit <sup>(3)</sup> .....            | Continuous                 |
| Operating Temperature .....                          | -55°C to +125°C            |
| Storage Temperature .....                            | -65°C to +150°C            |
| Junction Temperature .....                           | 150°C                      |
| Lead Temperature (soldering, 3s) .....               | 240°C                      |
| ESD Capability (Human Body Model) .....              | 4000V                      |

NOTES: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. (2) Input terminals are diode-clamped to the power supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current-limited to 10mA or less. (3) Short circuit to ground, one amplifier per package.



## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

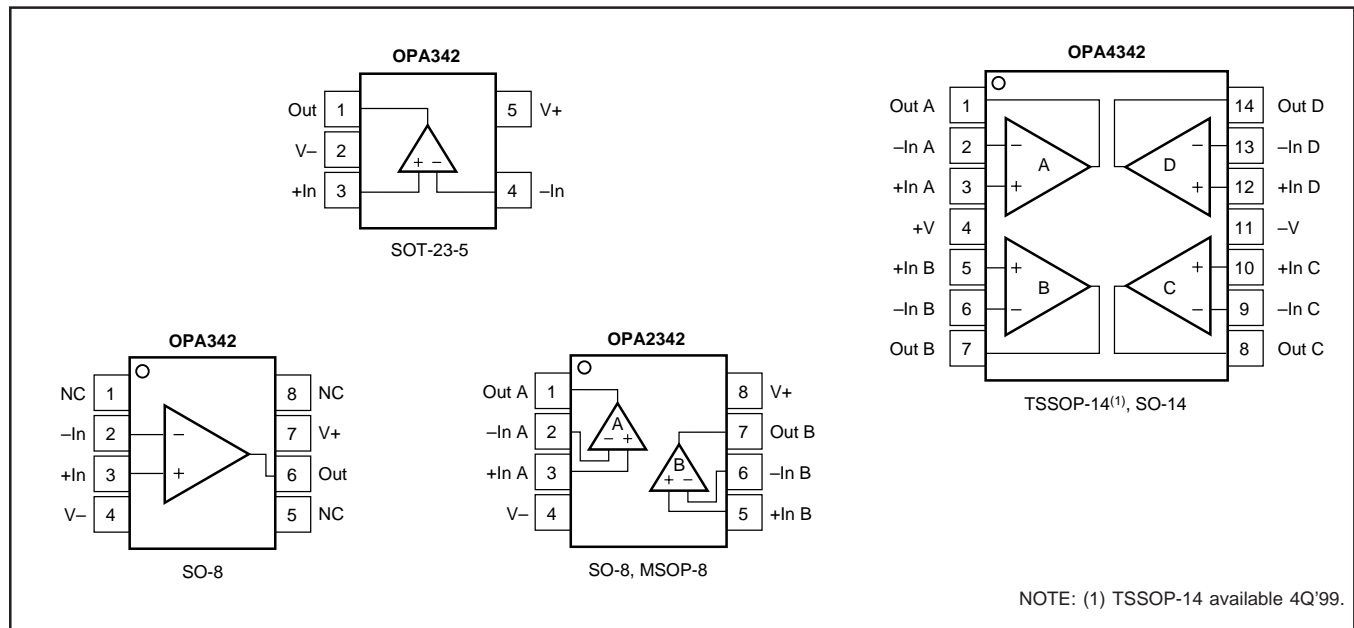
## PACKAGE/ORDERING INFORMATION

| PRODUCT         | PACKAGE       | PACKAGE DRAWING NUMBER <sup>(1)</sup> | SPECIFIED TEMPERATURE RANGE | PACKAGE MARKING | ORDERING NUMBER <sup>(2)</sup> | TRANSPORT MEDIA                |
|-----------------|---------------|---------------------------------------|-----------------------------|-----------------|--------------------------------|--------------------------------|
| OPA342NA<br>"   | SOT-23-5<br>" | 331<br>"                              | -40°C to +85°C<br>"         | B42<br>"        | OPA342NA/250<br>OPA342NA/3K    | Tape and Reel<br>Tape and Reel |
| OPA342UA<br>"   | SO-8<br>"     | 182<br>"                              | -40°C to +85°C<br>"         | OPA342UA<br>"   | OPA342UA<br>OPA342UA/2K5       | Rails<br>Tape and Reel         |
| OPA2342EA<br>"  | MSOP-8<br>"   | 337<br>"                              | -40°C to +85°C<br>"         | C42<br>"        | OPA2342EA/250<br>OPA2342EA/2K5 | Tape and Reel<br>Tape and Reel |
| OPA2342UA<br>"  | SO-8<br>"     | 182<br>"                              | -40°C to +85°C<br>"         | OPA2342UA<br>"  | OPA2342UA<br>OPA2342UA/2K5     | Rails<br>Tape and Reel         |
| OPA4342EA*<br>" | TSSOP-14<br>" | 357<br>"                              | -40°C to +85°C<br>"         | OPA4342EA<br>"  | OPA4342EA/250<br>OPA4342EA/2K5 | Tape and Reel<br>Tape and Reel |
| OPA4342UA<br>"  | SO-14<br>"    | 235<br>"                              | -40°C to +85°C<br>"         | OPA4342UA<br>"  | OPA4342UA<br>OPA4342UA/2K5     | Rails<br>Tape and Reel         |

NOTES: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /3K indicates 3000 devices per reel). Ordering 3000 pieces of "OPA342NA/3K" will get a single 3000-piece Tape and Reel. For detailed Tape and Reel mechanical information, refer to Appendix B of Burr-Brown IC Data Book.

\* OPA4342EA available 4Q'99.

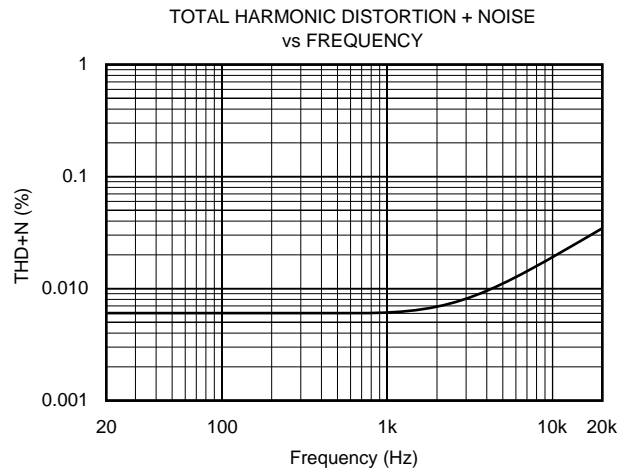
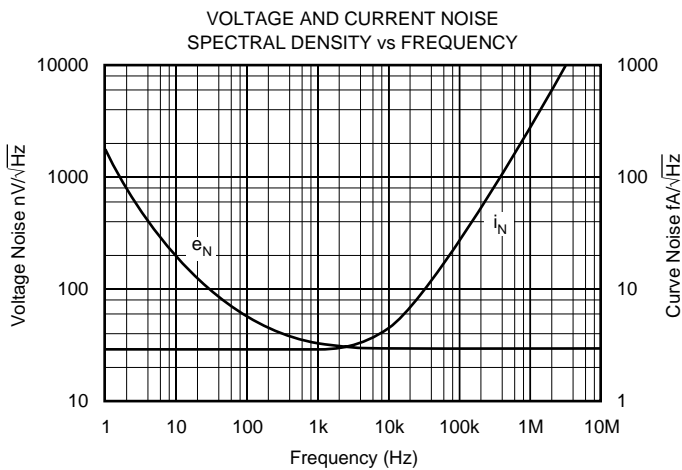
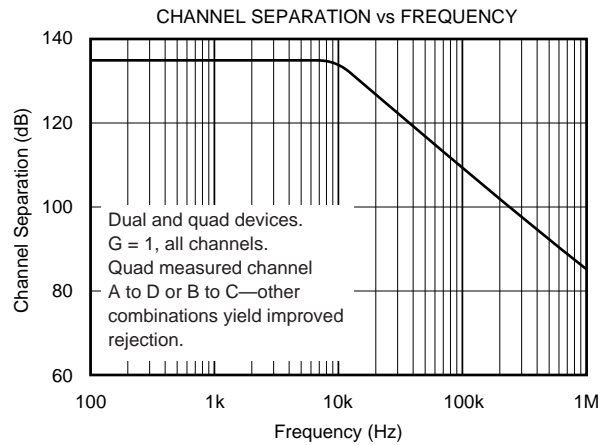
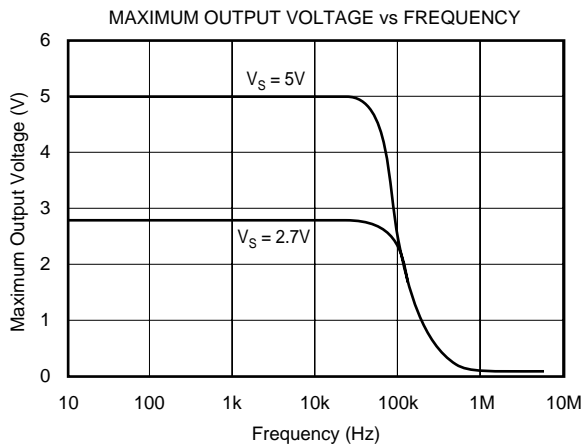
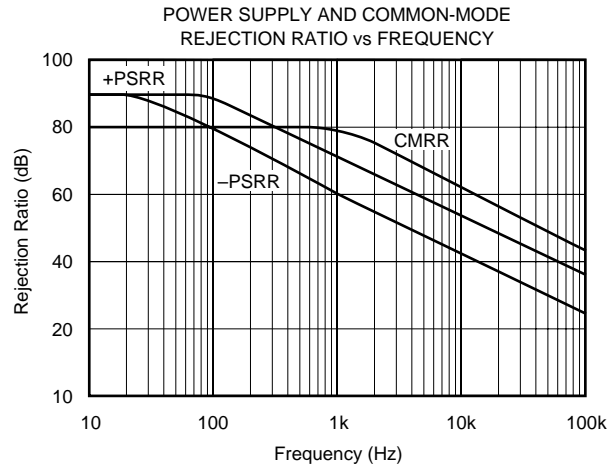
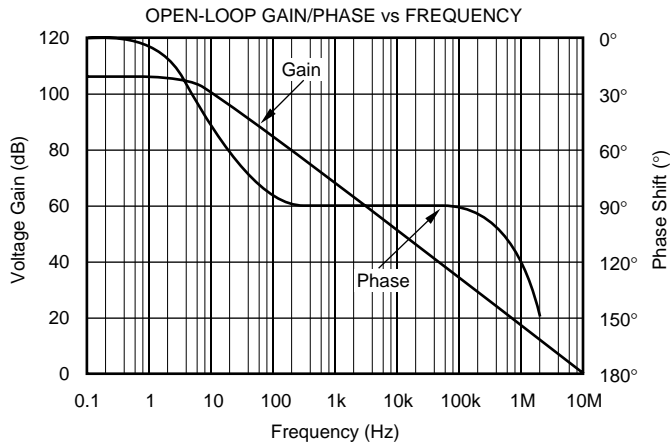
## PIN CONFIGURATIONS



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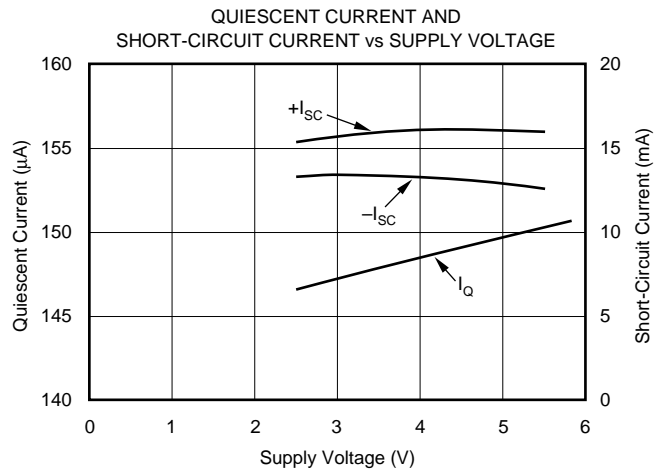
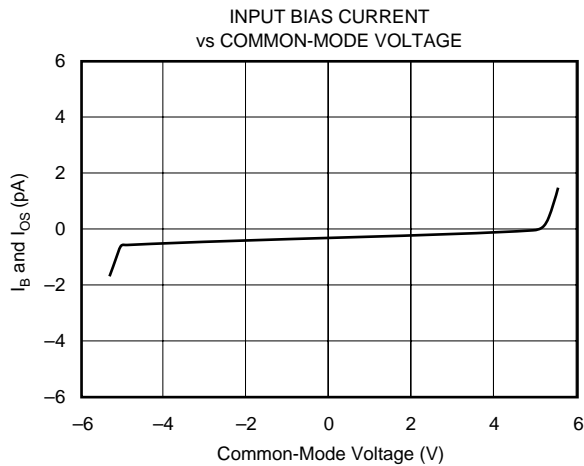
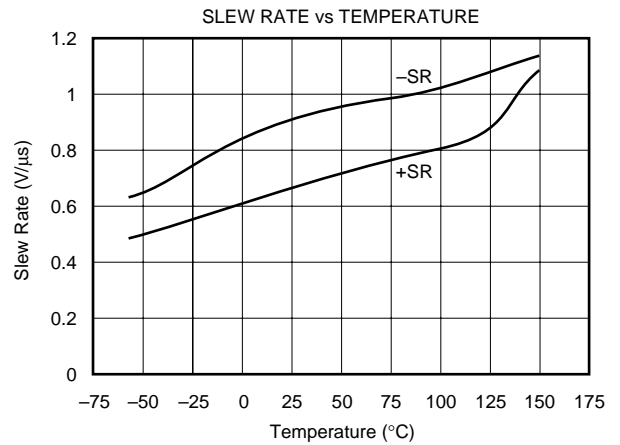
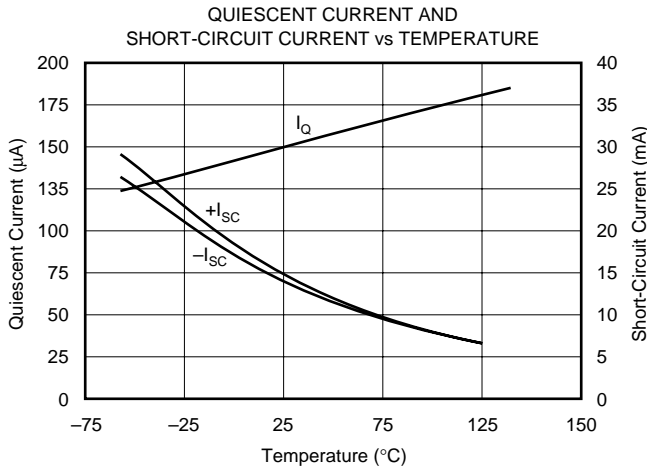
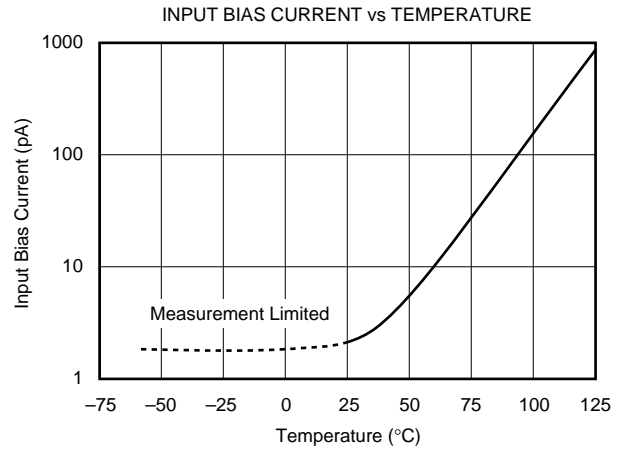
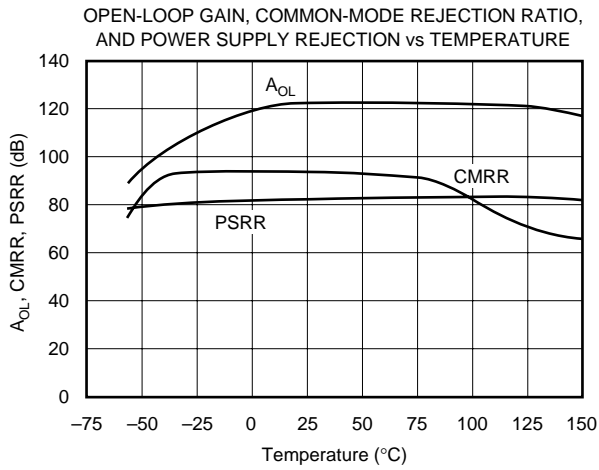
# TYPICAL PERFORMANCE CURVES

At  $T_A = +25^\circ\text{C}$ ,  $V_S = +5\text{V}$ , and  $R_L = 10\text{k}\Omega$ , unless otherwise noted.



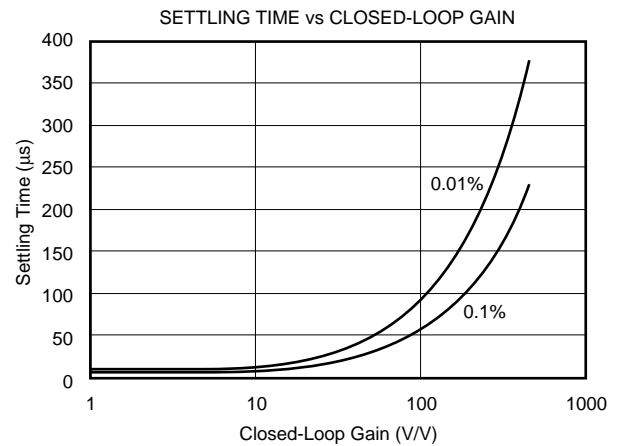
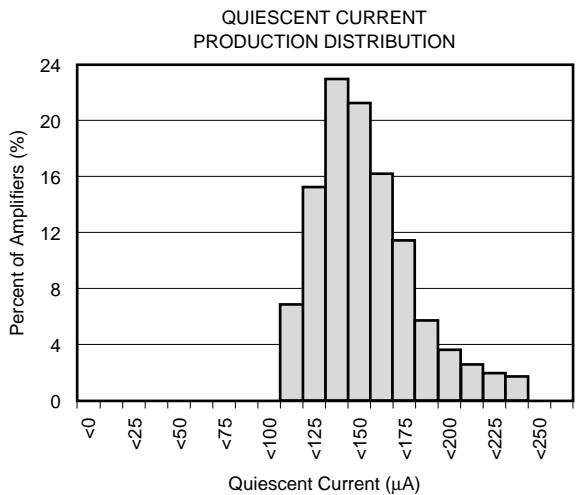
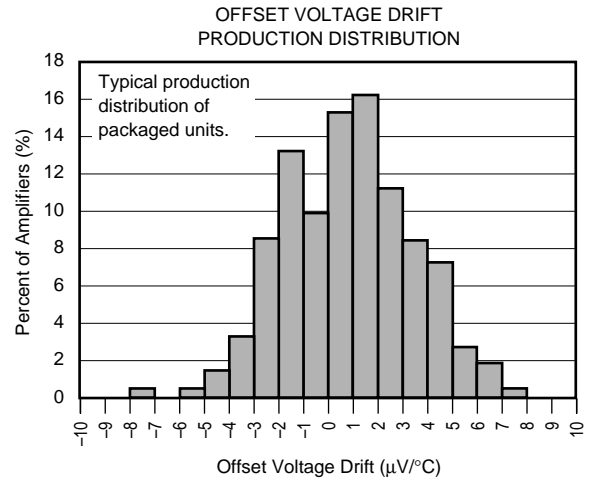
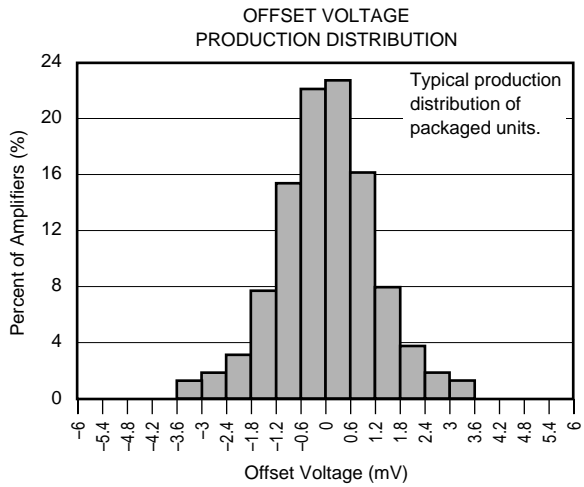
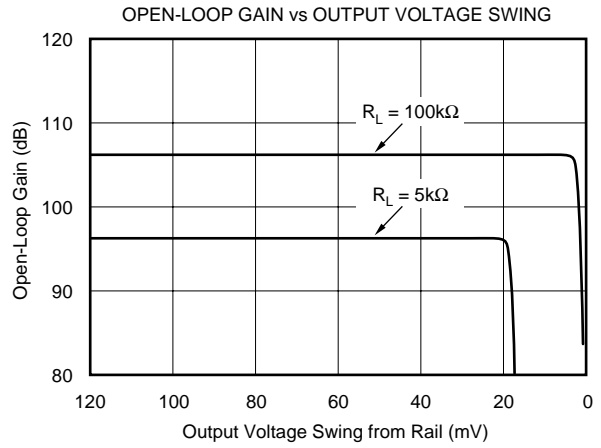
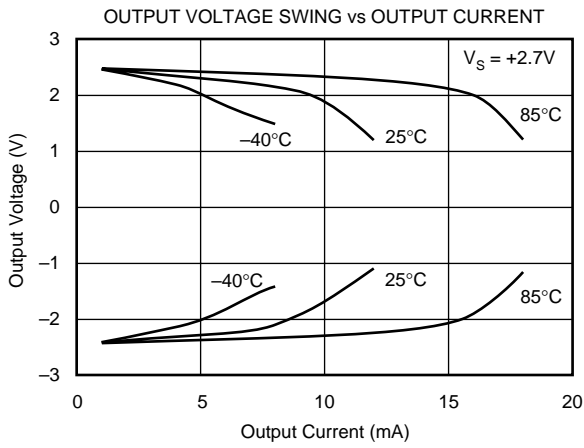
# TYPICAL PERFORMANCE CURVES (Cont.)

At  $T_A = +25^\circ\text{C}$ ,  $V_S = +5\text{V}$ , and  $R_L = 10\text{k}\Omega$ , unless otherwise noted.



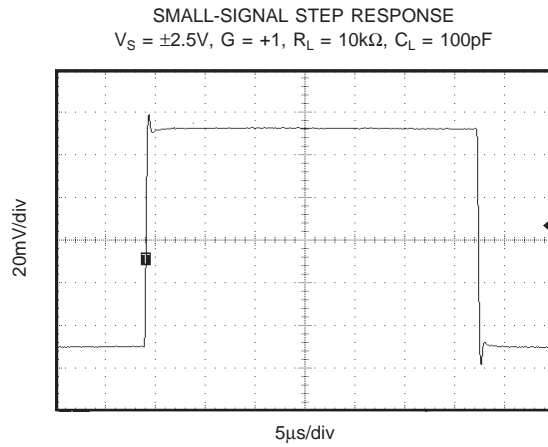
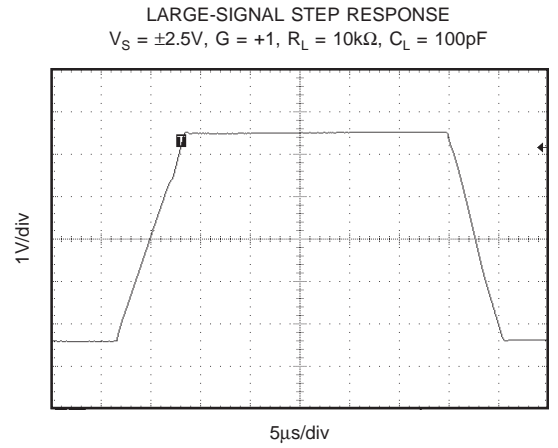
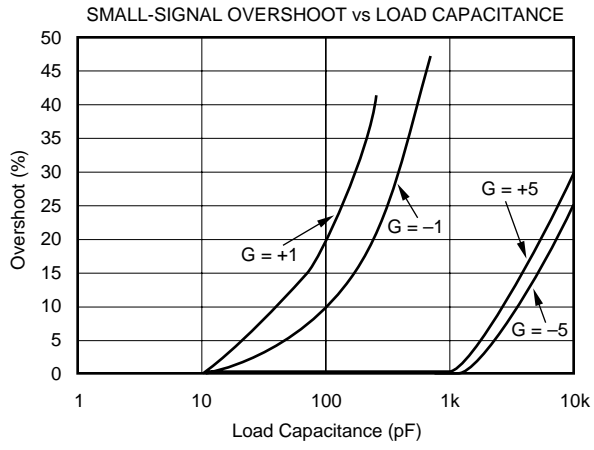
# TYPICAL PERFORMANCE CURVES (Cont.)

At  $T_A = +25^\circ\text{C}$ ,  $V_S = +5\text{V}$ , and  $R_L = 10\text{k}\Omega$ , unless otherwise noted.



# TYPICAL PERFORMANCE CURVES (Cont.)

At  $T_A = +25^\circ\text{C}$ ,  $V_S = +5\text{V}$ , and  $R_L = 10\text{k}\Omega$ , unless otherwise noted.



## APPLICATIONS INFORMATION

OPA342 series op amps are unity-gain stable and can operate on a single supply, making them highly versatile and easy to use.

Rail-to-rail input and output swing significantly increases dynamic range, especially in low supply applications. Figure 1 shows the input and output waveforms for the OPA342 in unity-gain configuration. Operation is from  $\pm 2.5\text{V}$  supplies with a  $10\text{k}\Omega$  load connected to ground. The input is a  $5\text{Vp-p}$  sinusoid. Output voltage is approximately  $4.997\text{Vp-p}$ .

Power supply pins should be bypassed with  $0.01\mu\text{F}$  ceramic capacitors.

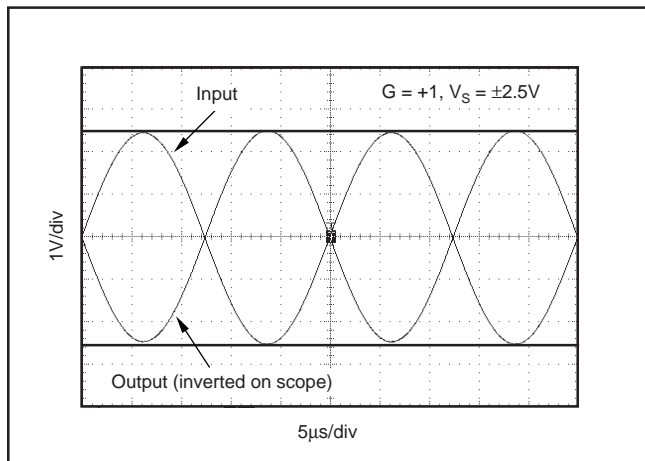


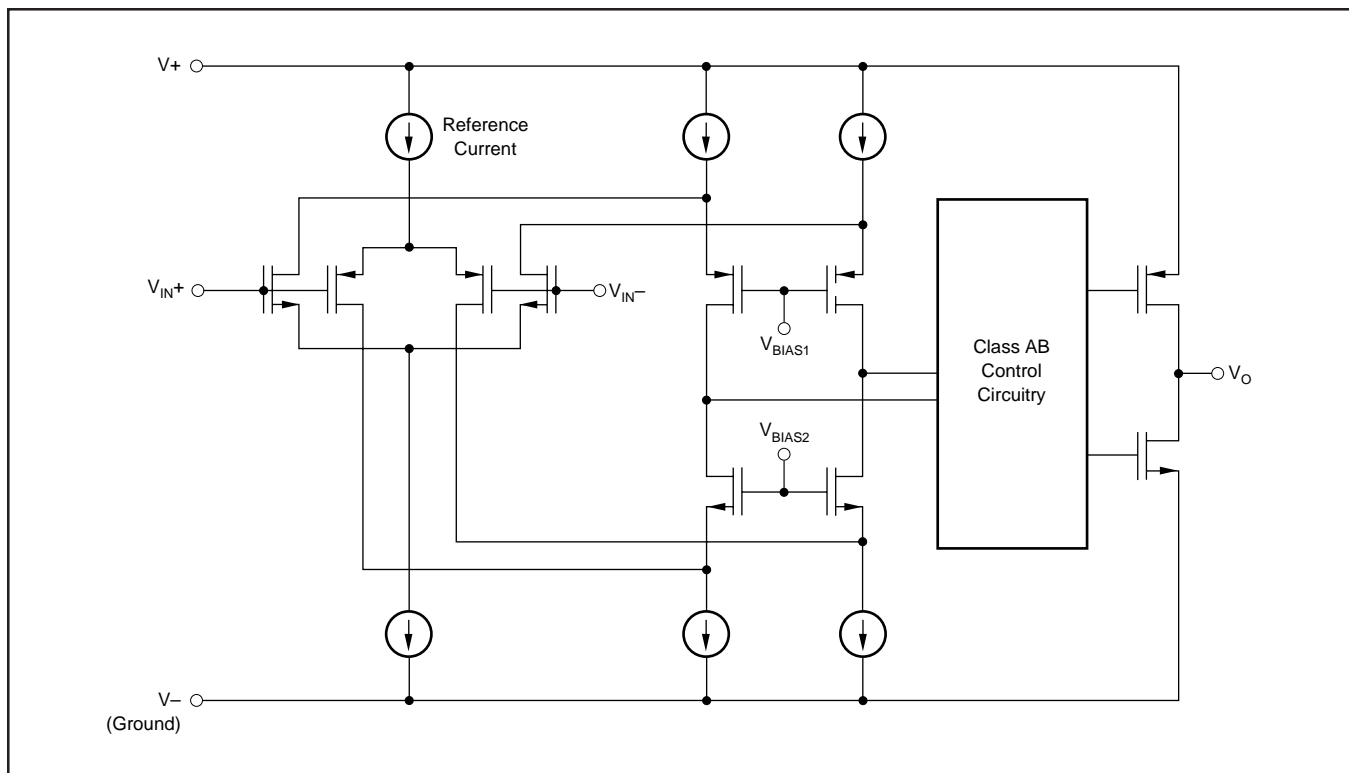
FIGURE 1. Rail-to-Rail Input and Output, Gain = +1.

## OPERATING VOLTAGE

OPA342 series op amps are fully specified and guaranteed from  $+2.7\text{V}$  to  $+5.5\text{V}$ . In addition, many specifications apply from  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ . Parameters that vary significantly with operating voltages or temperature are shown in the Typical Performance Curves.

## RAIL-TO-RAIL INPUT

The input common-mode voltage range of the OPA342 series extends  $300\text{mV}$  beyond the supply rails. This is achieved with a complementary input stage—an N-channel input differential pair in parallel with a P-channel differential pair (see Figure 2). The N-channel input pair is active for input voltages close to the positive rail, typically  $(V+) - 1.3\text{V}$  to  $300\text{mV}$  above the positive supply, while the P-channel input pair is active for inputs from  $300\text{mV}$  below the negative supply to approximately  $(V+) - 1.3\text{V}$ . There is a small transition region, typically  $(V+) - 1.5\text{V}$  to  $(V+) - 1.1\text{V}$ , in which both pairs are on. This  $400\text{mV}$  transition region can vary  $\pm 300\text{mV}$  with process variation. Thus, the transition region (both stages on) can range from  $(V+) - 1.8\text{V}$  to  $(V+) - 1.4\text{V}$  on the low end, up to  $(V+) - 1.2\text{V}$  to  $(V+) - 0.8\text{V}$  on the high end. Within the  $400\text{mV}$  transition region PSRR, CMRR, offset voltage, offset drift, and THD may be degraded compared to operation outside this region. For more information on designing with rail-to-rail input op amps, see Figure 3 “Design Optimization with Rail-to-Rail Input Op Amps.”





## COMMON-MODE REJECTION

The CMRR for the OPA342 is specified in several ways so the best match for a given application may be used. First, the CMRR of the device in the common-mode range below the transition region ( $V_{CM} < (V+) - 1.8V$ ) is given. This specification is the best indicator of the capability of the device when the application requires use of one of the differential input pairs. Second, the CMRR at 5.5V over the entire common-mode range is specified. Third, the CMRR at 2.7V over the entire common-mode range is provided. These last two values include the variations seen through the transition region.

## RAIL-TO-RAIL OUTPUT

A class AB output stage with common-source transistors is used to achieve rail-to-rail output. This output stage is capable of driving  $600\Omega$  loads connected to any point between  $V+$  and ground. For light resistive loads ( $> 50k\Omega$ ), the output voltage can typically swing to within 1mV from the supply rail. With moderate resistive loads ( $2k\Omega$  to  $50k\Omega$ ), the output can swing to within a few tens of millivolts from the supply rails while maintaining high open-loop gain. See the typical performance curve “Output Voltage Swing vs Output Current.”

## INPUT PROTECTION

Device inputs are protected by ESD diodes that will conduct if the input voltages exceed the power supplies by more than 300mV. Momentary voltages greater than 300mV beyond the power supply can be tolerated if the current on the input pins is limited to 10mA. This is easily accomplished with an input resistor as shown in Figure 4. Many input signals are inherently current-limited to less than 10mA, therefore, a limiting resistor is not required.

## CAPACITIVE LOAD AND STABILITY

The OPA342 series op amps in unity-gain configuration can drive up to 250pF pure capacitive load. Increasing the gain

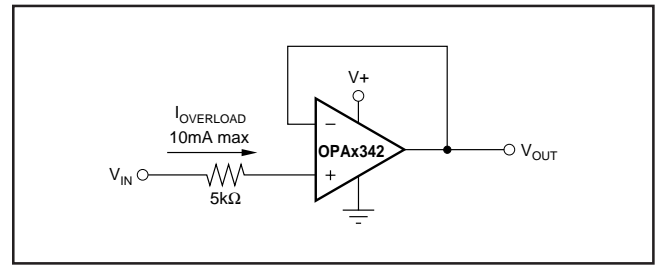


FIGURE 4. Input Current Protection for Voltages Exceeding the Supply Voltage.

enhances the amplifier’s ability to drive greater capacitive loads. See the typical performance curve “Small-Signal Overshoot vs Capacitive Load.”

In unity-gain configurations, capacitive load drive can be improved by inserting a small ( $10\Omega$  to  $20\Omega$ ) resistor  $R_S$  in series with the output, as shown in Figure 5. This significantly reduces ringing while maintaining dc performance for purely capacitive loads. However, if there is a resistive load in parallel with the capacitive load, a voltage divider is created, introducing a dc error at the output and slightly reducing the output swing. The error introduced is proportional to the ratio  $R_S/R_L$  and may be negligible.

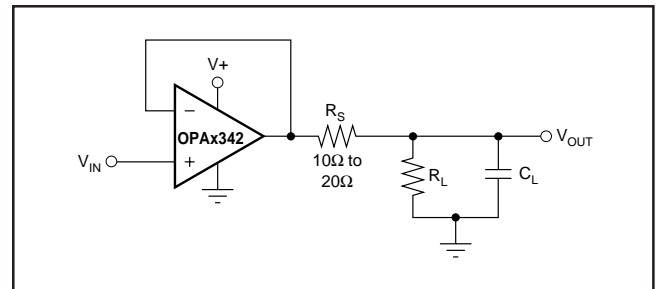


FIGURE 5. Series Resistor in Unity-Gain Configuration Improves Capacitive Load Drive.

## DESIGN OPTIMIZATION WITH RAIL-TO-RAIL INPUT OP AMPS

In most applications, operation is within the range of only one differential pair. However, some applications can subject the amplifier to a common-mode signal in the transition region. Under this condition, the inherent mismatch between the two differential pairs may lead to degradation of the CMRR and THD. The unity-gain buffer configuration is the most problematic—it will traverse through the transition region if a sufficiently

wide input swing is required. A design option would be to configure the op amp as a unity-gain inverter as shown below and hold the noninverting input at a set common-mode voltage outside the transition region. This can be accomplished with a voltage divider from the supply. The voltage divider should be designed such that the biasing point for the noninverting input is outside the transition region.

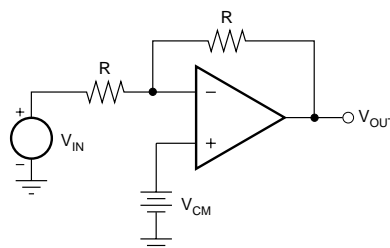


FIGURE 3. Design Optimization.

## DRIVING A/D CONVERTERS

OPA342 series op amps are optimized for driving medium speed sampling A/D converters. The OPA342 series provides an effective means of buffering the A/D's input capacitance and resulting charge injection while providing signal gain.

Figure 6 shows the OPA342 in a basic noninverting configuration driving the ADS7822. The ADS7822 is a 12-bit, micro-power sampling converter in the tiny MSOP-8 package. When used with the low power, mini-

ature packages of the OPA342, the combination is ideal for space-limited and low-power applications. In this configuration, an RC network at the A/D's input can be used to filter charge injection.

Figure 7 shows the OPA2342 driving an ADS7822 in a speech bandpass filtered data acquisition system. This small, low-cost solution provides the necessary amplification and signal conditioning to interface directly with an Electret microphone. This circuit will operate with +2.7V to +5V at less than 500 $\mu$ A quiescent current.

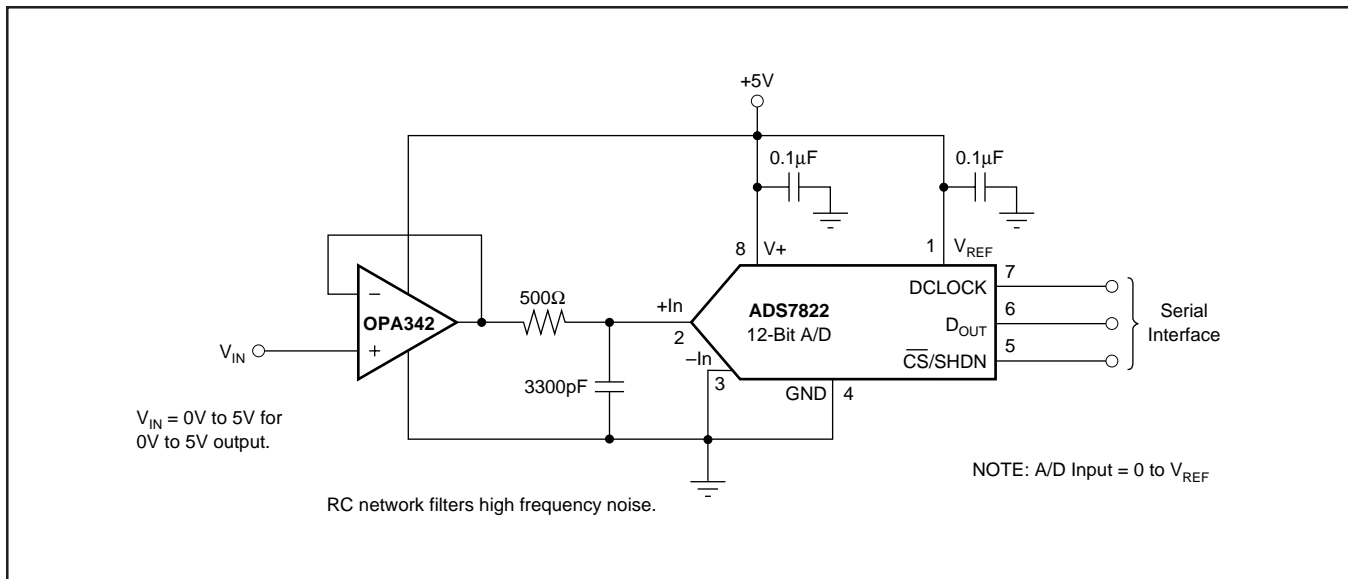


FIGURE 6. OPA342 in Noninverting Configuration Driving ADS7822.

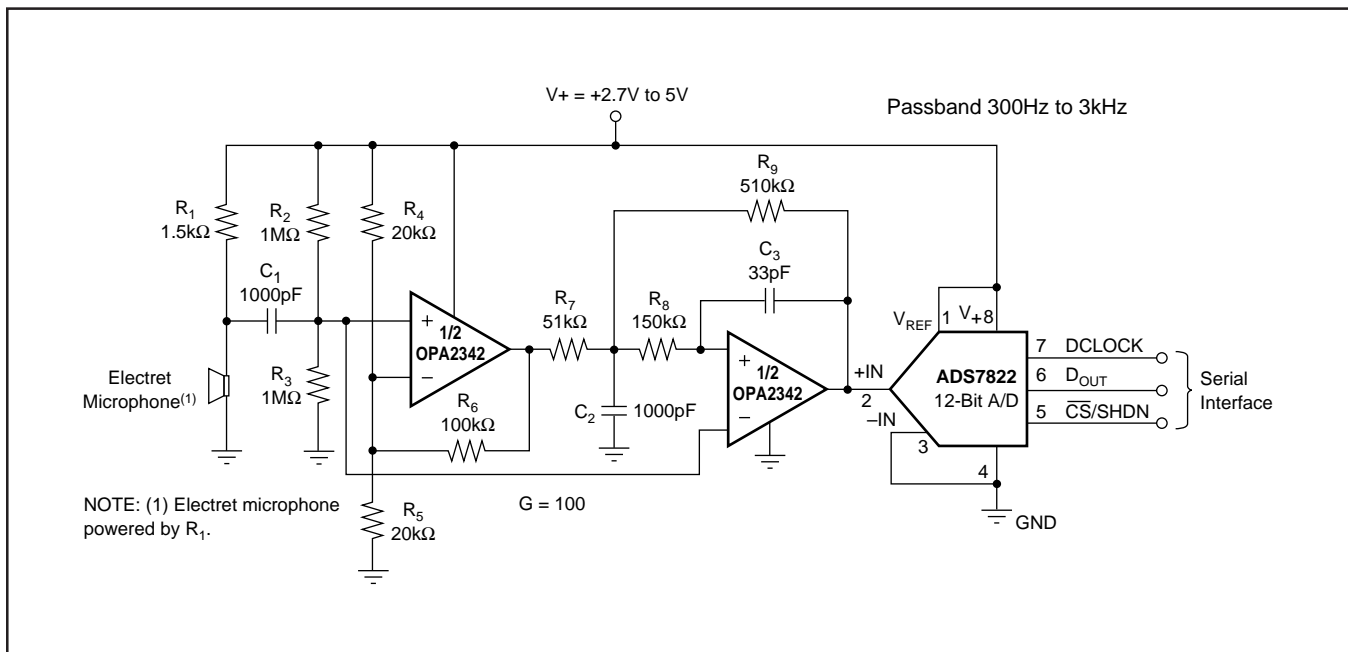


FIGURE 7. Speech Bandpass Filtered Data Acquisition System.

## INFLUENCE OF COMMON-MODE REJECTION ON OFFSET VOLTAGE

The offset voltage ( $V_{OS}$ ) of the OPA342 is guaranteed to be within  $\pm 6\text{mV}$  over the power supply range 2.7V to 5.5V with the common-mode voltage at  $V_S/2$ . This specification can be combined with the common-mode rejection ratio specification to determine worst-case offset under the conditions of a given application.

Common-Mode Rejection Ratio (CMRR) is specified in dB, which can be converted to  $\mu\text{V}/\text{V}$  using the equation:

$$\text{CMRR (in V/V)} = 10^{[(\text{CMRR in dB})/-20]} \quad (1)$$

For the OPA342, the worst-case CMRR at 5.5V supply over the full common-mode range is 66dB, or approximately  $501\mu\text{V}/\text{V}$ . This means that for every volt of change in common-mode, the offset could shift up to approximately  $501\mu\text{V}$ .

These numbers can be used to calculate excursions from the specified offset voltage under different application conditions. For example, a common application might configure the amplifier with a +5.5V single supply with 0V common-mode. This configuration varies from the

specified offset measurement configuration, representing a 2.75V variation in common-mode voltage ( $V_S/2 = 2.75\text{V}$  in the specification versus 0V in the application).

Calculation of the worst-case expected offset would be as follows:

$$\begin{aligned} \text{Worst Case } V_{OS} = & \\ & \text{Maximum specified } V_{OS} + \\ & (\text{common-mode variation} \cdot \text{CMRR}) \end{aligned} \quad (2)$$

$$\begin{aligned} V_{OSWC} = & \\ & 6\text{mV} + \\ & (2.75\text{V} \cdot 501\mu\text{V}/\text{V}) \\ & = \pm 7.38\text{mV} \end{aligned}$$

For the OPA342, a specification is also provided for power supply rejection. This information is useful for established expected offset variations in applications with varying supply voltage. Because the OPA342 offset is guaranteed over the full supply range, power supply rejection errors do not need to be factored into the worst-case offset analysis.