

## SINGLE-ENDED ANALOG-INPUT 20-BIT STEREO ANALOG-TO-DIGITAL CONVERTER

### FEATURES

- Dual 20-Bit Monolithic  $\Delta\Sigma$  ADC
- Single-Ended Voltage Input
- 64× Oversampling Decimation Filter:
  - Pass-Band Ripple:  $\pm 0.05$  dB
  - Stop-Band Attenuation:  $-65$  dB
- High Performance:
  - THD+N:  $-88$  dB (typical)
  - SNR: 95 dB (typical)
  - Dynamic Range: 95 dB (typical)
  - Internal High-Pass Filter
- PCM Audio Interface:
  - Master/Slave Modes
  - Four Data Formats
- Sampling Rate: 4 kHz to 48 kHz
- System Clock: 256  $f_s$ , 384  $f_s$ , or 512  $f_s$
- Single 5-V Power Supply
- Small 24-Pin SSOP Package

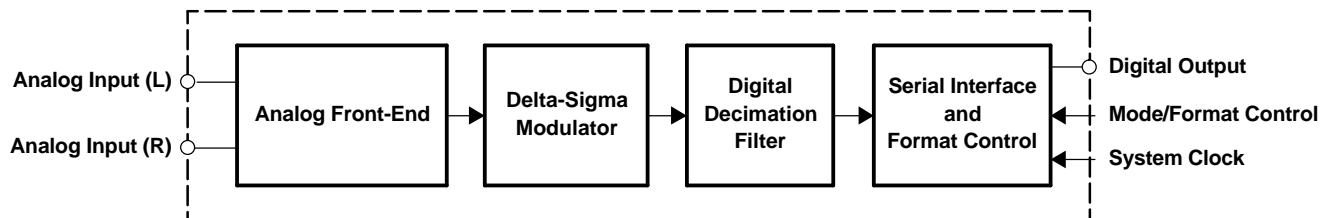
### APPLICATIONS

- DVD Recorders
- DVD Receivers
- AV Amplifier Receivers
- Electric Musical Instruments

### DESCRIPTION

The PCM1800 is a low-cost, single-chip stereo analog-to-digital converter (ADC) with single-ended analog voltage inputs. The PCM1800 uses a delta-sigma modulator with 64 times oversampling, including a digital decimation filter and a serial interface which supports both master and slave modes and four data formats. The PCM1800 is suitable for a wide variety of cost-sensitive consumer applications where good performance is required.

The PCM1800 is fabricated using a highly advanced CMOS process and is available in a small 24-pin SSOP package.



B0003-01



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

System Two, Audio Precision are trademarks of Audio Precision, Inc.  
All other trademarks are the property of their respective owners.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ELECTRICAL CHARACTERISTICS

All specifications at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = V_{CC} = 5\text{ V}$ , slave mode,  $f_S = 44.1\text{ kHz}$ , 20-bit input data, and  $\text{SYSCLK} = 384 f_S$ , unless otherwise noted

PARAMETER	TEST CONDITIONS	PCM1800E			UNITS
		MIN	TYP	MAX	
<b>RESOLUTION</b>		20			Bits
<b>DIGITAL INPUT/OUTPUT</b>					
$V_{IH}^{(1)}$	Input logic level	2			VDC
$V_{IL}^{(1)}$				0.8	
$I_{IN}^{(2)}$	Input logic current			$\pm 1$	$\mu\text{A}$
$I_{IN}^{(3)}$				100	
$V_{OH}^{(4)}$	Output logic level	$I_{OH} = -1.6\text{ mA}$	4.5		VDC
$V_{OL}^{(4)}$		$I_{OL} = 3.2\text{ mA}$		0.5	
$f_S$	Sampling frequency	4	44.1	48	kHz
	System clock frequency	$256 f_S$	1.024	11.2896	12.288
		$384 f_S$	1.536	16.9344	18.432
		$512 f_S$	2.048	22.5792	24.576
<b>DC ACCURACY</b>					
	Gain mismatch, channel-to-channel		$\pm 1$	$\pm 2.5$	% of FSR
	Gain error		$\pm 2$	$\pm 5$	% of FSR
	Gain drift		$\pm 20$		ppm of FSR/ $^\circ\text{C}$
	Bipolar zero error	High-pass filter bypassed	$\pm 2$		% of FSR
	Bipolar zero drift	High-pass filter bypassed	$\pm 20$		ppm of FSR/ $^\circ\text{C}$
<b>DYNAMIC PERFORMANCE<sup>(5)</sup></b>					
	THD+N at FS ( $-0.5\text{ dB}$ )		$-88$	$-80$	dB
	THD+N at $-60\text{ dB}$		$-92$		dB
	Dynamic range	A-weighted	90	95	dB
	Signal-to-noise ratio	A-weighted	90	95	dB
	Channel separation		88	93	dB
<b>DYNAMIC PERFORMANCE<sup>(5)</sup></b>					
	Dynamic range	16-bit, A-weighted		94	dB
	Signal-to-noise ratio	16-bit, A-weighted		94	dB
	Channel separation	16-bit		92	dB

(1) Pins 6, 7, 8, 9, 10, 11, 16 and 12, 13, 14: RSTB, BYPAS, FMT0, FMT1, MODE0, MODE1, SYSCLK, and FSYNC, LRCK, BCK in slave mode

(2) Pins 16 and 12, 13, 14: SYSCLK and FSYNC, LRCK, BCK in slave mode (Schmitt-trigger input)

(3) Pins 6, 7, 8, 9, 10, 11: RSTB, BYPAS, FMT0, FMT1, MODE0, MODE1 (Schmitt-trigger input, with  $100\text{-k}\Omega$  typical pulldown resistor)

(4) Pins 15 and 12, 13, 14: DOUT and FSYNC, LRCK, BCK in master mode

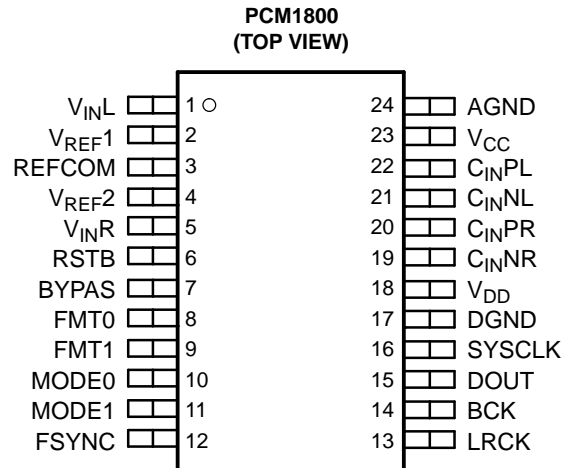
(5)  $f_{IN} = 1\text{ kHz}$ , using the System Two™ audio measurement system by Audio Precision™, rms mode with  $20\text{-kHz}$  LPF and  $400\text{-Hz}$  HPF in the performance calculation.

**ELECTRICAL CHARACTERISTICS (continued)**

All specifications at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = V_{CC} = 5\text{ V}$ , slave mode,  $f_S = 44.1\text{ kHz}$ , 20-bit input data, and  $\text{SYSCLK} = 384 f_S$ , unless otherwise noted

PARAMETER	TEST CONDITIONS	PCM1800E			UNITS	
		MIN	TYP	MAX		
<b>ANALOG INPUT</b>						
Input range	FS ( $V_{IN} = 0\text{ dB}$ )		2.828		Vp-p	
Center voltage			2.1		VDC	
Input impedance			30		k $\Omega$	
Antialiasing filter frequency response	$C_{EXT} = 470\text{ pF}$ , $-3\text{ dB}$		170		kHz	
<b>DIGITAL FILTER PERFORMANCE</b>						
Pass band				$0.454 f_S$	Hz	
Stop band		$0.583 f_S$			Hz	
Pass-band ripple				$\pm 0.05$	dB	
Stop-band attenuation		$-65$			dB	
Delay time (latency)			$17.4/f_S$		s	
High-pass frequency response	$-3\text{ dB}$		$0.019 f_S$		mHz	
<b>POWER SUPPLY REQUIREMENTS</b>						
$V_{CC}$	Voltage range		4.5	5	5.5	VDC
$V_{DD}$			4.5	5	5.5	
	Supply current <sup>(6)</sup>	$V_{CC} = V_{DD} = 5\text{ V}$		18	25	mA
	Power dissipation	$V_{CC} = V_{DD} = 5\text{ V}$		90	125	mW
<b>TEMPERATURE RANGE</b>						
$T_A$	Operation		$-25$		85	$^\circ\text{C}$
$T_{stg}$	Storage		$-55$		125	$^\circ\text{C}$
$\theta_{JA}$	Thermal resistance			100		$^\circ\text{C/W}$

(6) No load on DOUT (pin 15) in the slave mode

**PIN CONFIGURATION**

P0004-01

**PIN ASSIGNMENTS**

NAME	PIN	I/O	DESCRIPTION
AGND	24	–	Analog ground
BCK	14	I/O	Bit clock input/output
BYPAS	7	I	High-pass filter bypass control <sup>(1)</sup>
$C_{INNL}$	21	–	Antialias filter capacitor (–), Lch
$C_{INNR}$	19	–	Antialias filter capacitor (–), Rch
$C_{INPL}$	22	–	Antialias filter capacitor (+), Lch
$C_{INPR}$	20	–	Antialias filter capacitor (+), Rch
DGND	17	–	Digital ground
DOUT	15	O	Audio data output
FMT0	8	I	Audio data format 0 <sup>(1)</sup>
FMT1	9	I	Audio data format 1 <sup>(1)</sup>
FSYNC	12	I/O	Frame synchronization, input/output
LRCK	13	I/O	Sampling clock input/output ( $f_S$ )
MODE0	10	I	Master/slave mode selection 0 <sup>(1)</sup>
MODE1	11	I	Master/slave mode selection 1 <sup>(1)</sup>
REFCOM	3	–	Reference decoupling common
SYSCLK	16	I	System clock input, 256 $f_S$ , 384 $f_S$ , or 512 $f_S$
RSTB	6	I	Reset input, active LOW <sup>(1)</sup>
$V_{CC}$	23	–	Analog power supply
$V_{DD}$	18	–	Digital power supply
$V_{INL}$	1	I	Analog input, Lch
$V_{INR}$	5	I	Analog input, Rch
$V_{REF1}$	2	–	Reference 1 decoupling capacitor
$V_{REF2}$	4	–	Reference 2 decoupling capacitor

(1) With 100-k $\Omega$  typical pulldown resistor

**PACKAGE/ORDERING INFORMATION**

PRODUCT	PACKAGE TYPE	PACKAGE CODE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA	QUANTITY
PCM1800E	24-pin SSOP	DB	PCM1800E	PCM1800E	Rails	58
				PCM1800E/2K	Tape and reel	2000

**ABSOLUTE MAXIMUM RATINGS**

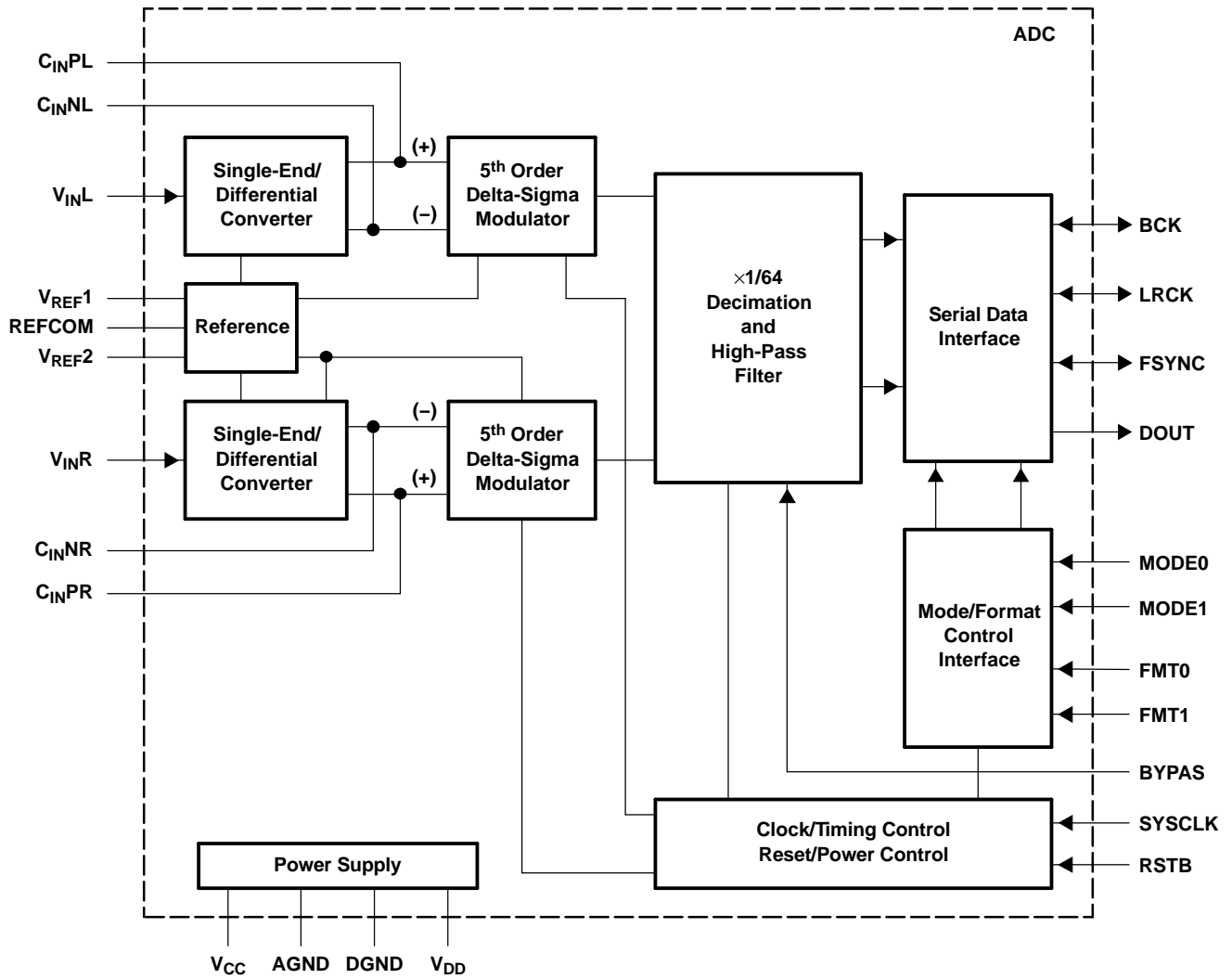
Supply voltage: $V_{DD}$ , $V_{CC}$	–0.3 V to 6.5 V
Supply voltage differences	±0.1 V
GND voltage differences	±0.1 V
Digital input voltage	–0.3 V to ( $V_{DD} + 0.3$ V), < 6.5 V
Analog input voltage	–0.3 V to ( $V_{CC} + 0.3$ V), < 6.5 V
Input current (any pin except supplies)	±10 mA
Power dissipation	300 mW
Operating temperature range	–25°C to 85°C
Storage temperature	–55°C to 125°C
Lead temperature, soldering	260°C, 5 s
Package temperature (IR reflow, peak)	235°C

**RECOMMENDED OPERATING CONDITIONS**

over operating free-air temperature range (unless otherwise noted)

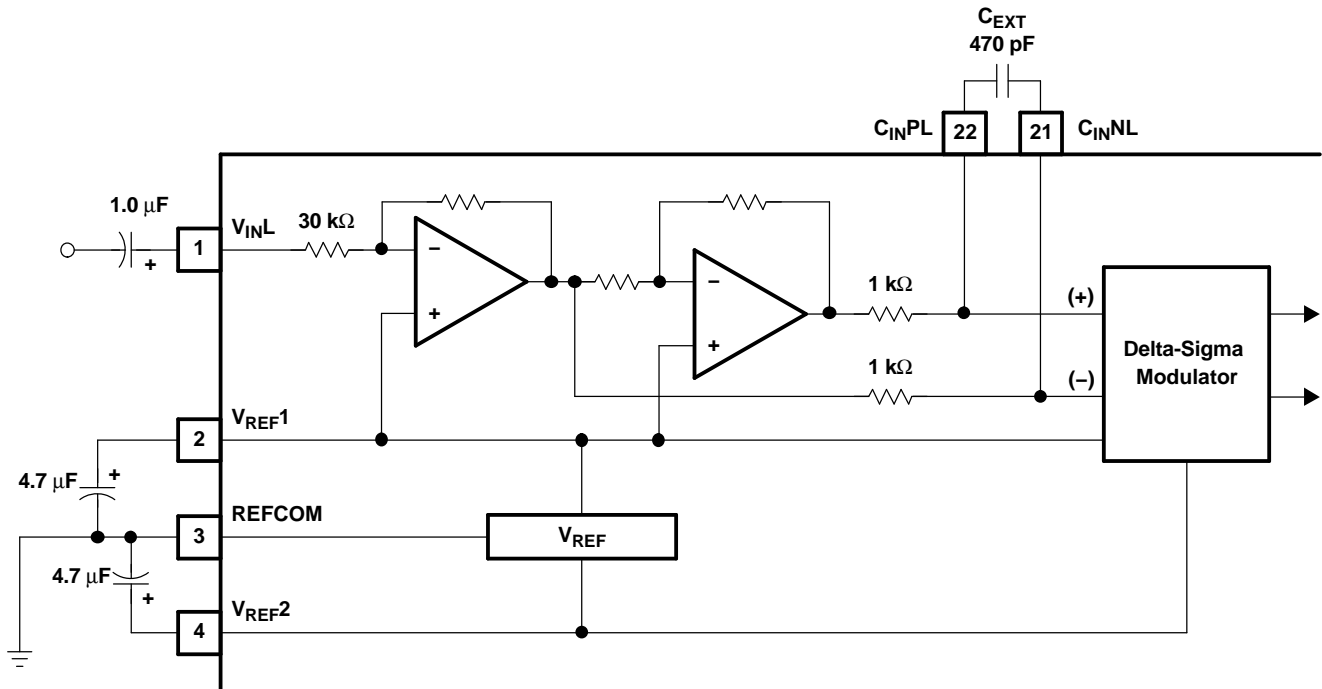
		MIN	NOM	MAX	UNIT
Analog supply voltage, $V_{CC}$		4.5	5	5.5	V
Digital supply voltage, $V_{DD}$		4.5	5	5.5	V
Analog input voltage, full-scale (–0 dB)		2.828			Vp-p
Digital input logic family		TTL			
Digital input clock frequency	System clock	8.192	24.576		MHz
	Sampling clock	32	48		kHz
Digital output load capacitance		10			pF
Operating free-air temperature, $T_A$		–25	85		°C

BLOCK DIAGRAM



B0004-01

**ANALOG FRONT-END (Single Channel)**



S0011-01

**TYPICAL PERFORMANCE CURVES**

All specifications at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = V_{CC} = 5\text{ V}$ , slave mode,  $f_S = 44.1\text{ kHz}$ , 20-bit input data, and  $\text{SYSCLK} = 384 f_S$ , unless otherwise noted

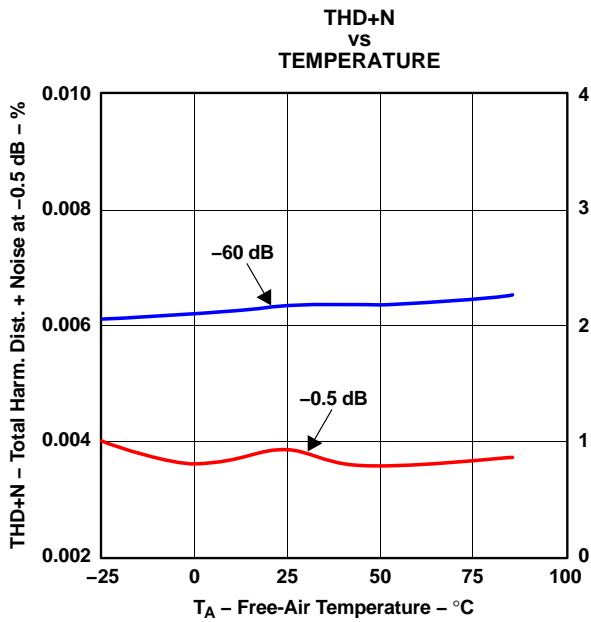


Figure 1.

G001

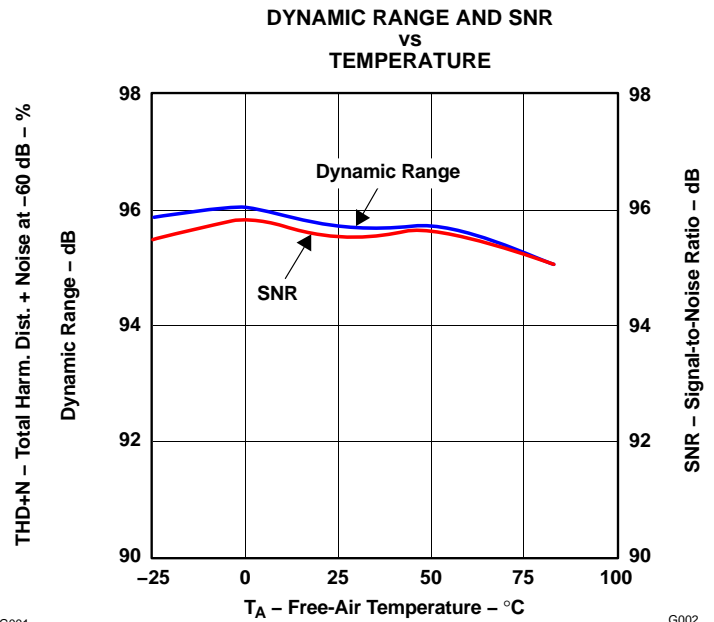


Figure 2.

G002

**TYPICAL PERFORMANCE CURVES (continued)**

All specifications at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = V_{CC} = 5\text{ V}$ , slave mode,  $f_S = 44.1\text{ kHz}$ , 20-bit input data, and  $\text{SYSCLK} = 384 f_S$ , unless otherwise noted

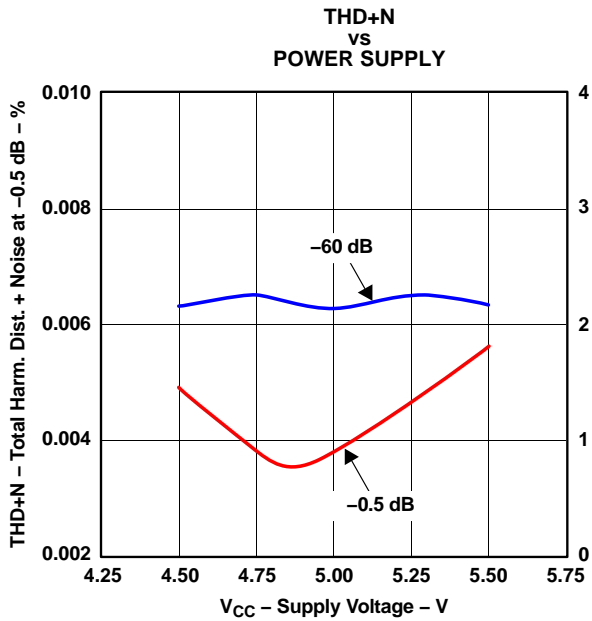


Figure 3.

G003

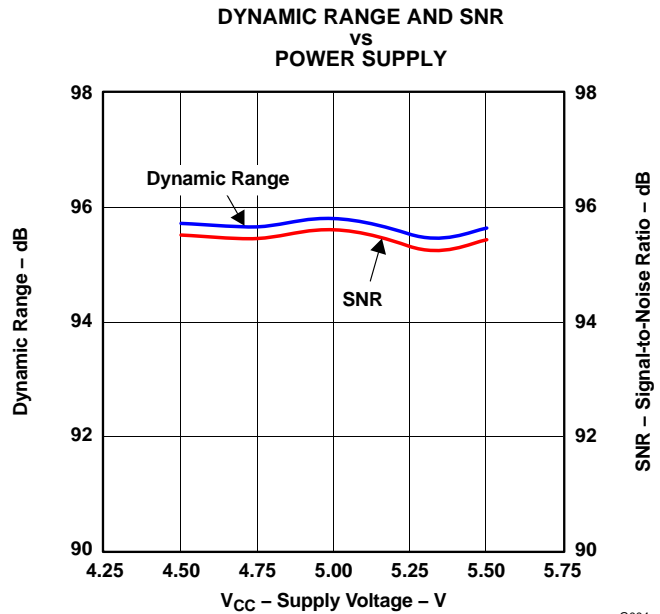


Figure 4.

G004

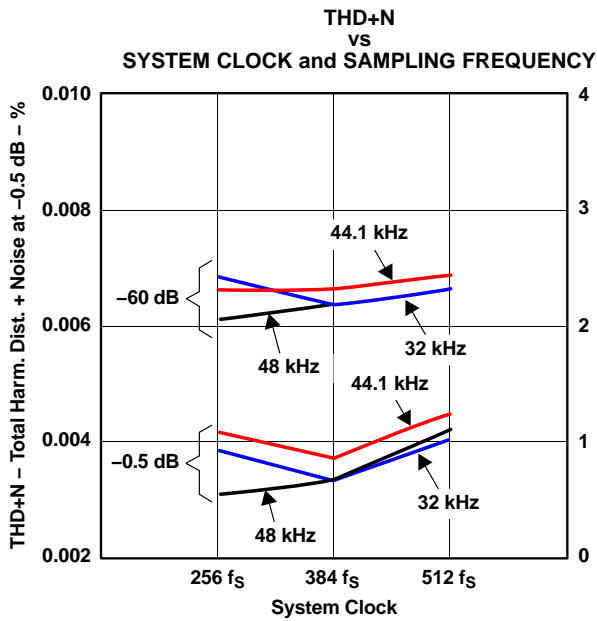


Figure 5.

G005

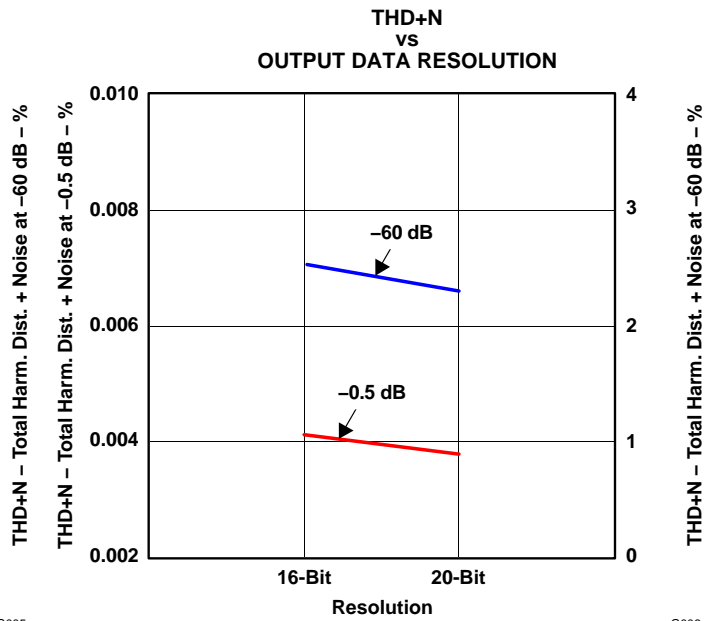


Figure 6.

G006



**TYPICAL PERFORMANCE CURVES (continued)**

All specifications at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = V_{CC} = 5\text{ V}$ , slave mode,  $f_S = 44.1\text{ kHz}$ , 20-bit input data, and  $\text{SYSCLK} = 384 f_S$ , unless otherwise noted

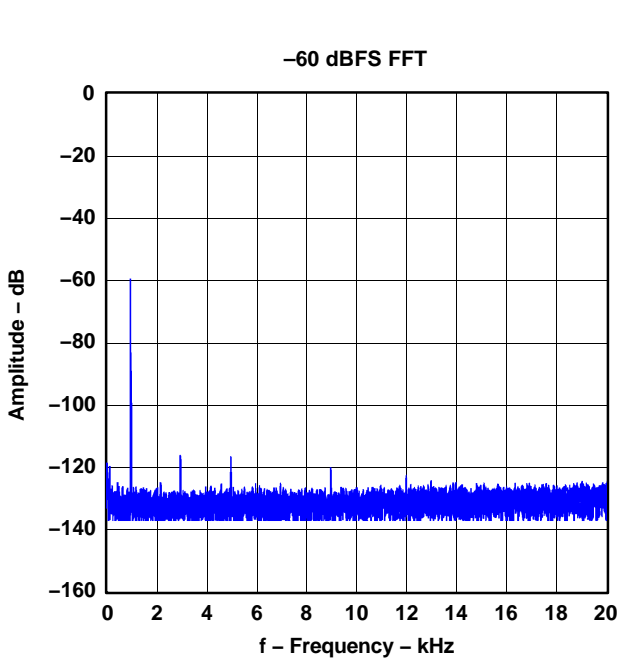


Figure 7.

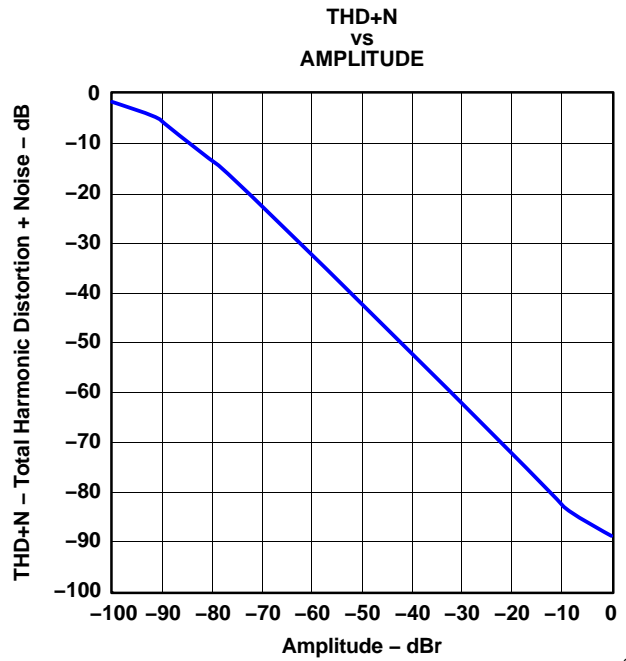


Figure 8.

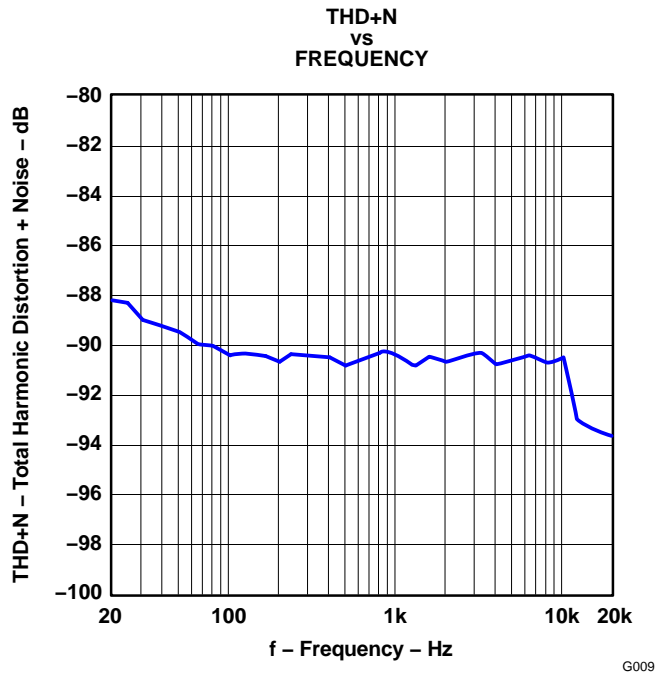


Figure 9.

TYPICAL PERFORMANCE CURVES FOR INTERNAL FILTERS

DECIMATION FILTER

OVERALL CHARACTERISTICS

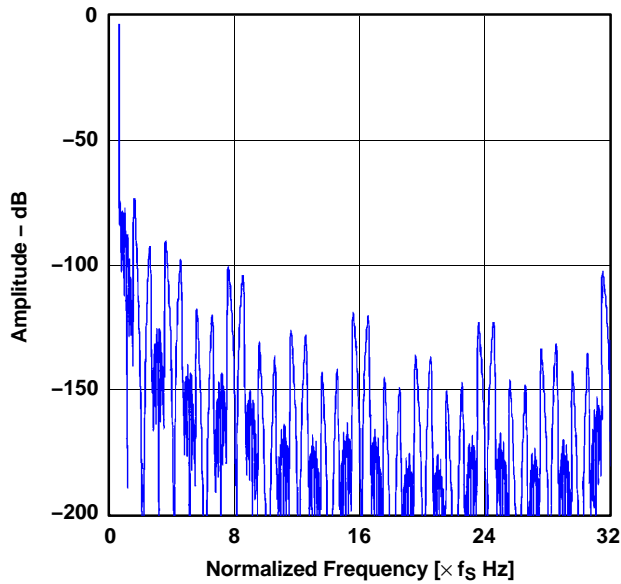


Figure 10.

G010

STOP-BAND ATTENUATION CHARACTERISTICS

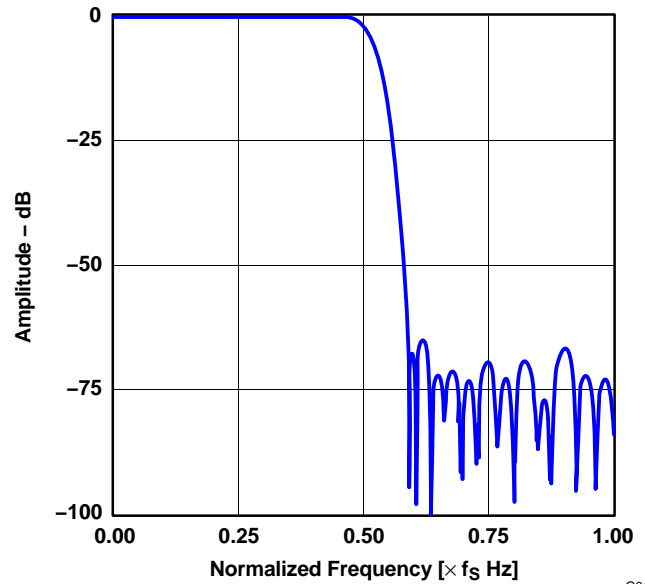


Figure 11.

G011

PASS-BAND RIPPLE CHARACTERISTICS

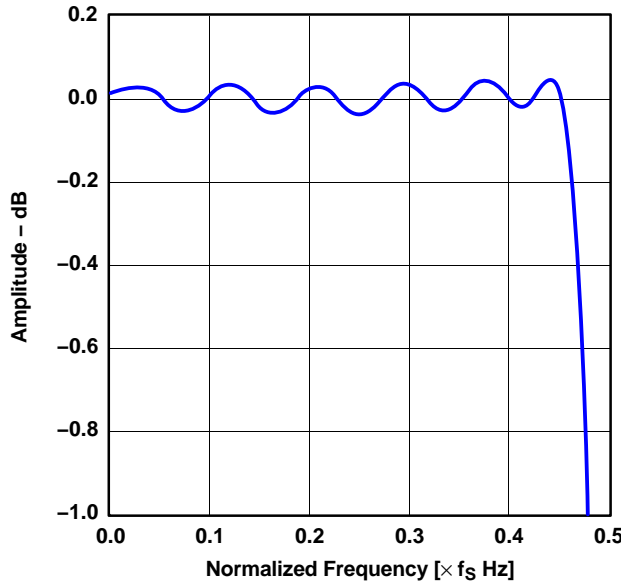


Figure 12.

G012

TRANSITION BAND CHARACTERISTICS

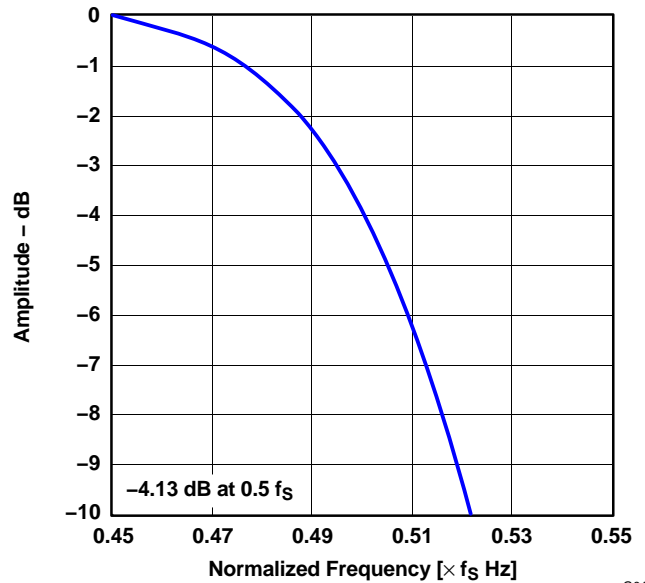


Figure 13.

G013

## TYPICAL PERFORMANCE CURVES FOR INTERNAL FILTERS (continued)

### HIGH-PASS FILTER

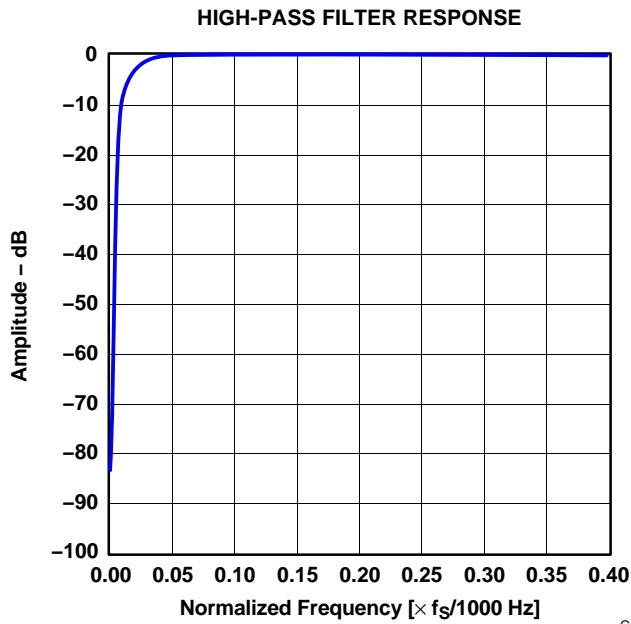


Figure 14.

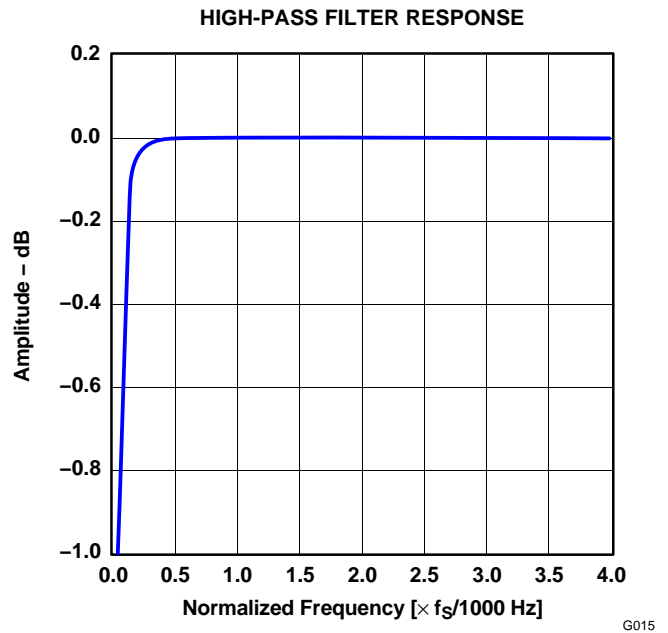


Figure 15.

### ANTI\_ALIASING FILTER

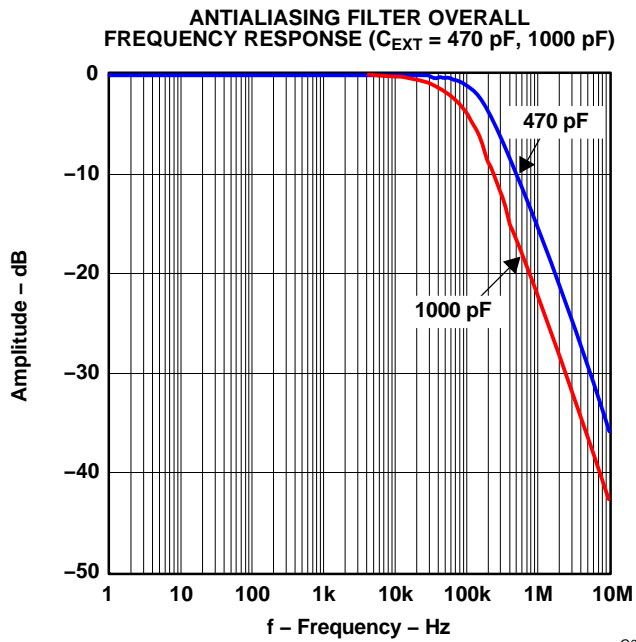


Figure 16.

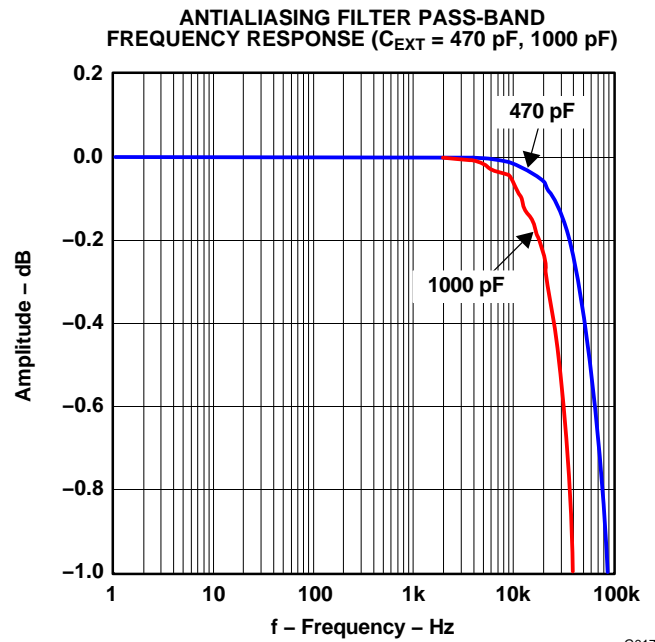


Figure 17.

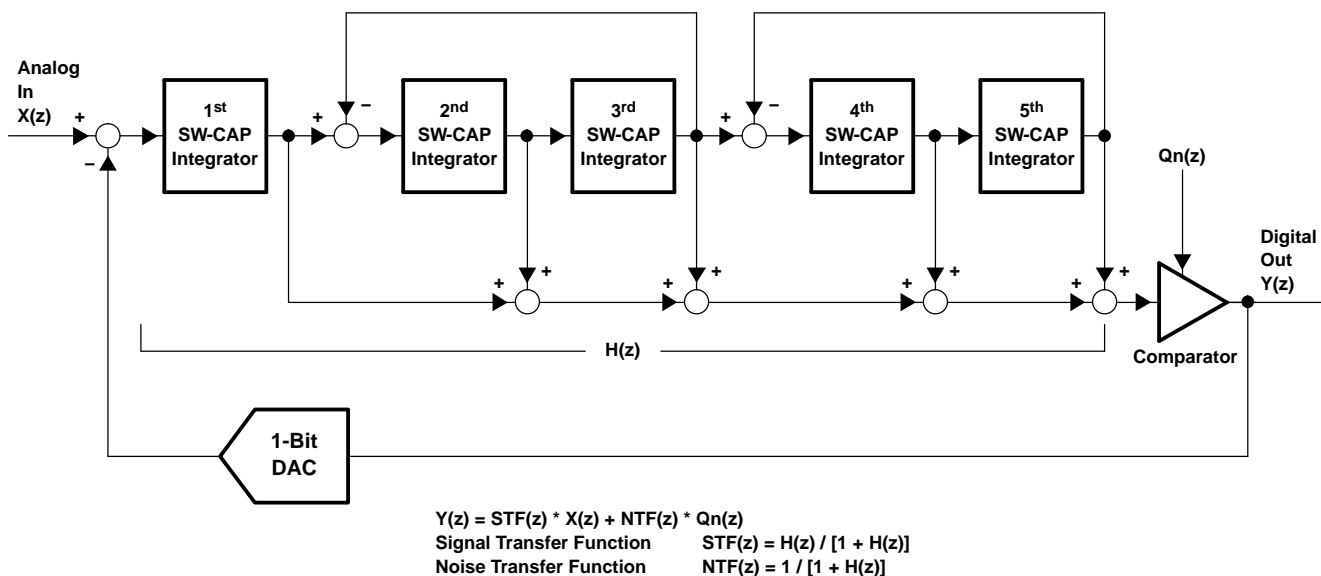
## THEORY OF OPERATION

The PCM1800 consists of a band-gap reference, two channels of a single-to-differential converter, a fully differential 5th-order delta-sigma modulator, a decimation filter (including digital high pass), and a serial interface circuit. The block diagram illustrates the total architecture of the PCM1800 and the analog front-end diagram illustrates the architecture of the single-to-differential converter and the antialiasing filter. Figure 18 illustrates the architecture of the 5th-order delta-sigma modulator and transfer functions.

An internal high-precision reference with two external capacitors provides all the reference voltages that are required by the converter, and defines the full-scale voltage range of both channels. The internal single-to-differential voltage converter saves the design, space, and extra parts needed for external circuitry required by many delta-sigma converters. The internal full-differential architecture provides a wide dynamic range and excellent power-supply rejection performance.

The input signal is sampled at a  $64\times$  oversampling rate, eliminating the need for a sample-and-hold circuit, and simplifying antialias filtering requirements. The 5th-order delta-sigma noise shaper consists of five integrators which use a switched-capacitor topology, a comparator, and a feedback loop consisting of a 1-bit DAC. The delta-sigma modulator shapes the quantization noise, shifting it out of the audio band in the frequency domain. The high order of the modulator enables it to randomize the modulator outputs, reducing idle tone levels.

The  $64\text{-}f_s$ , 1-bit stream from the modulator is converted to  $1\text{-}f_s$ , 20-bit digital data by the decimation filter, which also acts as a low-pass filter to remove the shaped quantization noise. The dc components are removed by a high-pass filter, and the filtered output is converted to time-multiplexed serial signals through a serial interface which provides flexible serial formats and master/slave modes.



B0005-01

Figure 18. Simplified Diagram of the PCM1800 5th-Order Delta-Sigma Modulator

## SYSTEM CLOCK

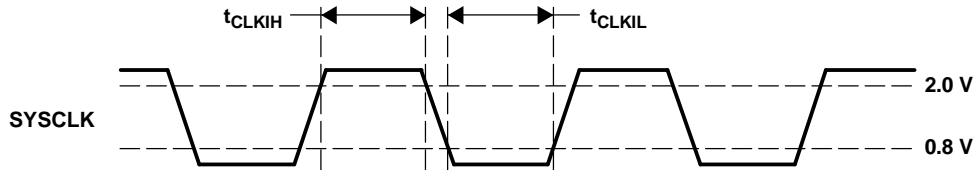
The system clock for the PCM1800 must be either  $256 f_s$ ,  $384 f_s$ , or  $512 f_s$ , where  $f_s$  is the audio sampling frequency. The system clock must be supplied on SYSCLK (pin 16).

The PCM1800 also has a system-clock detection circuit which automatically senses if the system clock is operating at  $256 f_s$ ,  $384 f_s$ , or  $512 f_s$ .

When the  $384\text{-}f_s$  or  $512\text{-}f_s$  system clock is in slave mode, the system clock is divided into  $256 f_s$  automatically. The  $256\text{-}f_s$  clock is used to operate the digital filter and the modulator. Table 1 lists the relationship of typical sampling frequencies and system clock frequencies. Figure 19 illustrates the system clock timing.

Table 1. System Clock Frequencies

SAMPLING RATE FREQUENCY (kHz)	SYSTEM CLOCK FREQUENCY (MHz)		
	256 $f_s$	384 $f_s$	512 $f_s$
32	8.1920	12.2880	16.3840
44.1	11.2896	16.9344	22.5792
48	12.2880	18.4320	24.5760



System clock pulse duration, HIGH	$t_{CLKIH}$	12 ns (min)
System clock pulse duration, LOW	$t_{CLKIL}$	12 ns (min)

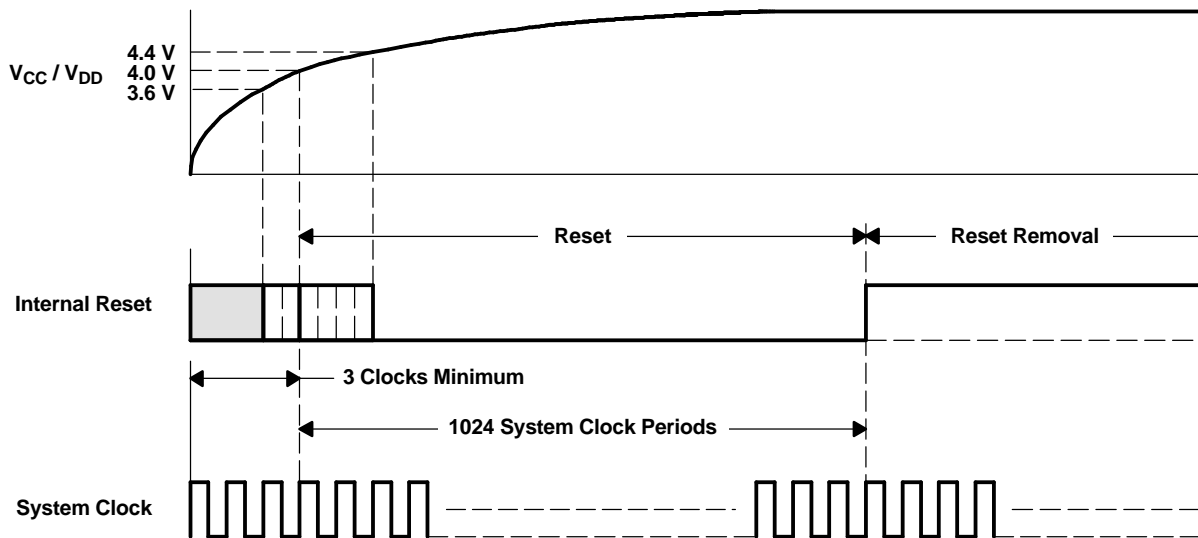
T0005-03

Figure 19. System Clock Timing

## RESET AND POWER DOWN

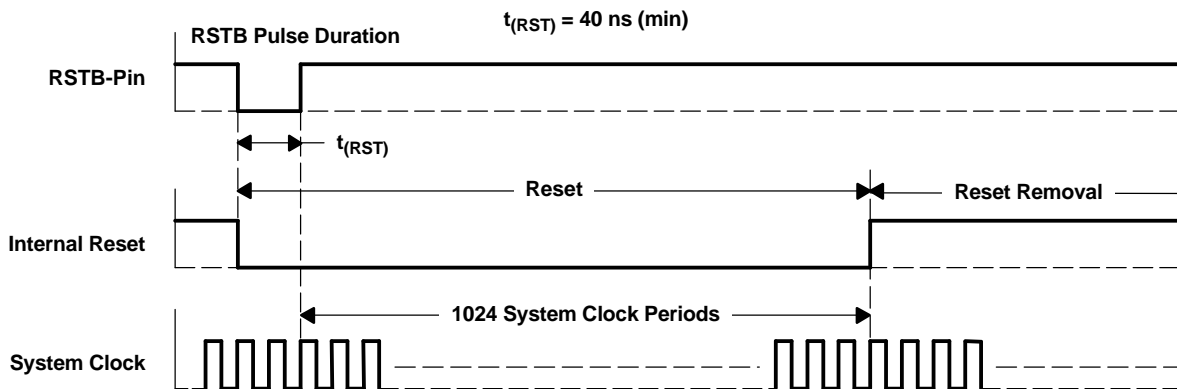
The PCM1800 has both an internal power-on reset circuit and an external forced reset (RSTB, pin 6). The internal power-on reset initializes (resets) when the supply voltage ( $V_{CC}/V_{DD}$ ) exceeds 4 V (typical). To initiate the reset sequence externally, apply a logic-level LOW to the RSTB pin.

The RSTB pin is terminated by an internal pulldown resistor. If the RSTB pin is unconnected, the ADC remains in the reset state. Because the system clock is used as the clock signal for the reset circuit, the system clock must be supplied as soon as power is applied; more specifically, the device must receive at least three system clock cycles before  $V_{DD} > 4$  V and RSTB = HIGH. If this system clock requirement cannot be assured in an application, RSTB must be held LOW until the system clock is supplied. While  $V_{CC}/V_{DD} < 4$  V (typical), RSTB = LOW, and for 1024 system clock periods after  $V_{CC}/V_{DD} > 4.0$  V and RSTB = HIGH, the PCM1800 stays in the reset state and the digital output is forced to zero. The digital output is valid 18,436  $f_s$  periods after release from the reset state. During reset, the logic circuits and the digital filter stop operating and enter the power-down mode. Figure 20 and Figure 21 illustrate the internal power-on reset and external reset timing.



T0014-01

Figure 20. Internal Power-On Reset Timing



T0015-01

Figure 21. RSTB-Pin Reset Timing

### SERIAL AUDIO DATA INTERFACE

The PCM1800 interfaces with the audio system through BCK (pin 14), LRCK (pin 13), FSYNC (pin 12), and DOUT (pin 15).

### INTERFACE MODE

The PCM1800 supports master and slave modes as interface modes, which are selected by MODE1 (pin 11) and MODE0 (pin 10), as shown in Table 2. When in master mode, the PCM1800 provides the timing for serial audio data communications between the PCM1800 and the digital audio processor or external circuit. When in slave mode, the PCM1800 receives the timing for data transfer from an external controller.

Table 2. Interface Mode

MODE1	MODE0	INTERFACE MODE
0	0	Slave mode (256/384/512 f <sub>S</sub> )
0	1	Master mode (512 f <sub>S</sub> )
1	0	Master mode (384 f <sub>S</sub> )
1	1	Master mode (256 f <sub>S</sub> )

### MASTER MODE

In master mode, BCK, LRCK, and FSYNC are output pins and are controlled by timing generated in the clock circuitry of the PCM1800.

FSYNC is used to designate the valid data from the PCM1800. The rising edge of FSYNC indicates the starting point of the converted audio data, and the following edge of this signal indicates the ending point of data. The frequency of this signal is fixed at 2× LRCK, and the duty-cycle ratio depends on the data bit length. The frequency of BCK is fixed at 64× LRCK.

### SLAVE MODE

In slave mode, BCK, LRCK, and FSYNC are input pins. FSYNC is used to enable the BCK signal, and the PCM1800 can shift out the converted data when FSYNC is HIGH.

### DATA FORMAT

The PCM1800 supports four audio data formats in both master and slave modes. These data formats are selected by FMT1 (pin 9) and FMT0 (pin 8), as shown in Table 3. Figure 22 and Figure 23 illustrate the data formats in slave mode and master mode, respectively.

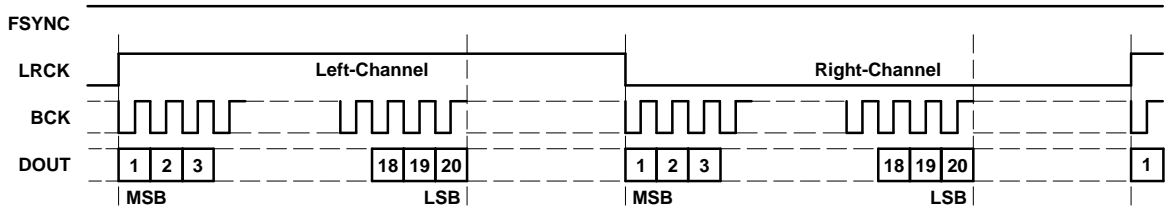
Table 3. Data Format

FORMAT NO.	FMT1 <sup>(1)</sup>	FMT0 <sup>(1)</sup>	DATA FORMAT
0	0	0	20-bit, left-justified
1	0	1	20-bit, I <sup>2</sup> S
2	1	0	16-bit, right-justified
3	1	1	20-bit, right-justified

(1) FMT1 and FMT0 must be stable when RSTB changes from LOW to HIGH.

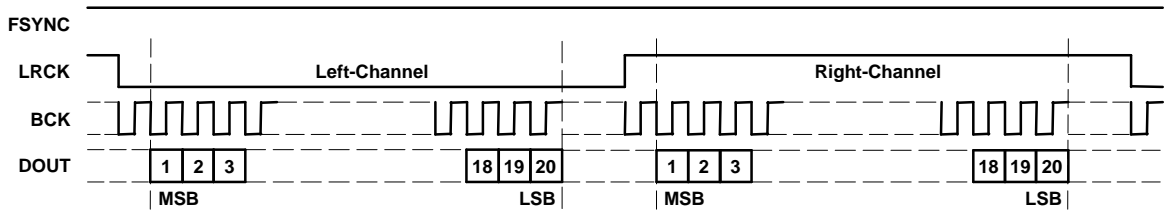
**FORMAT 0: FMT[1:0] = 00**

20-Bit, MSB-First, Left-Justified



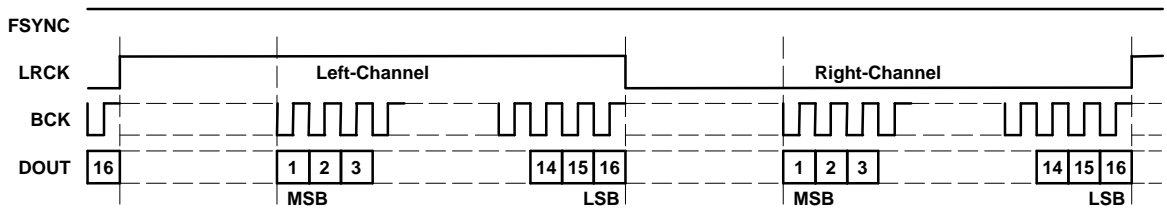
**FORMAT 1: FMT[1:0] = 01**

20-Bit, MSB-First, I<sup>2</sup>S



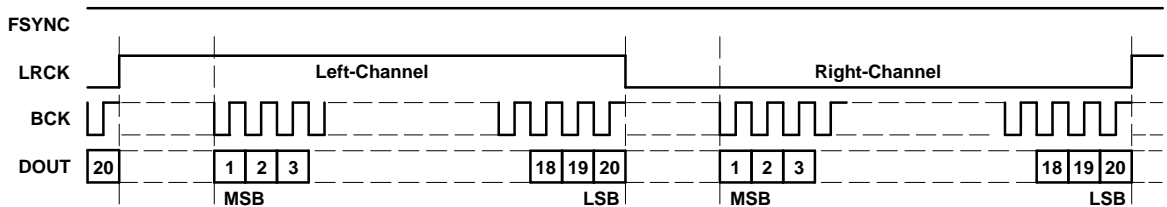
**FORMAT 2: FMT[1:0] = 10**

16-Bit, MSB-First, Right-Justified



**FORMAT 3: FMT[1:0] = 11**

20-Bit, MSB-First, Right-Justified

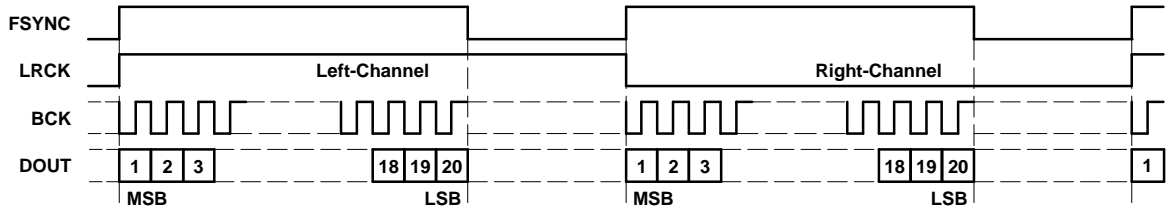


T0016-01

Figure 22. Audio Data Format (Slave Mode: FSYNC, LRCK, and BCK Are Inputs)

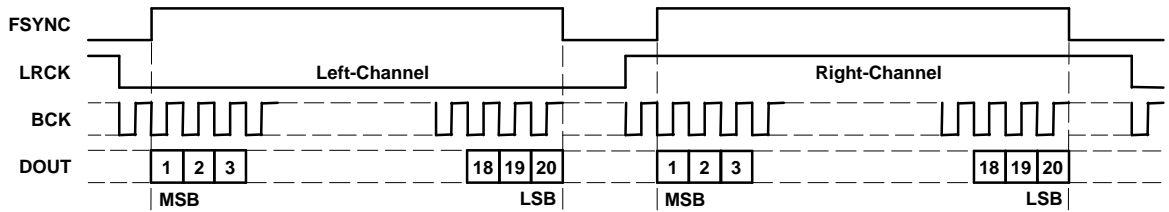
**FORMAT 0: FMT[1:0] = 00**

20-Bit, MSB-First, Left-Justified



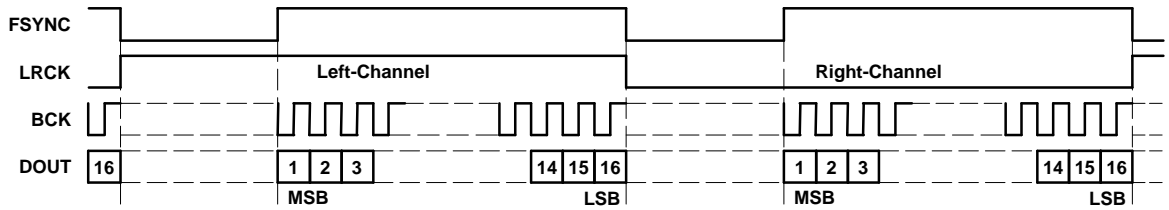
**FORMAT 1: FMT[1:0] = 01**

20-Bit, MSB-First, I<sup>2</sup>S



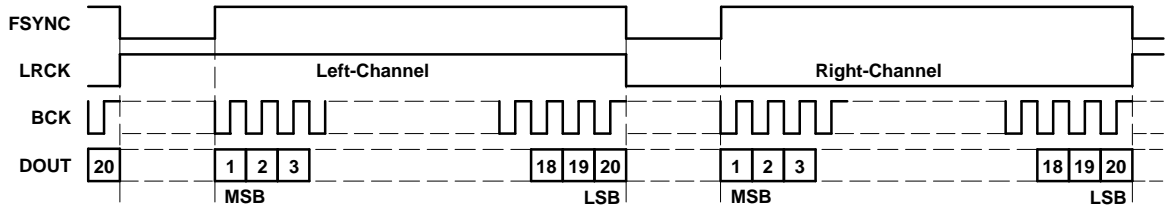
**FORMAT 2: FMT[1:0] = 10**

16-Bit, MSB-First, Right-Justified



**FORMAT 3: FMT[1:0] = 11**

20-Bit, MSB-First, Right-Justified



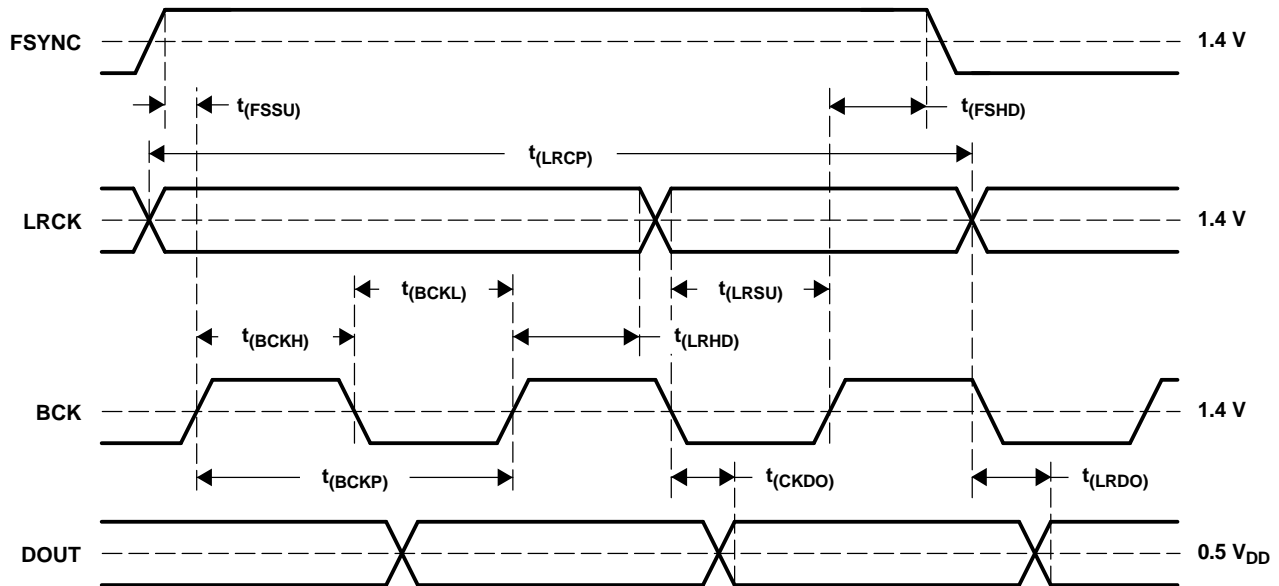
T0016-02

**Figure 23. Audio Data Format (Master Mode: FSYNC, LRCK, and BCK Are Outputs)**



## INTERFACE TIMING

Figure 24 and Figure 25 illustrate the interface timing in slave mode and master mode, respectively.

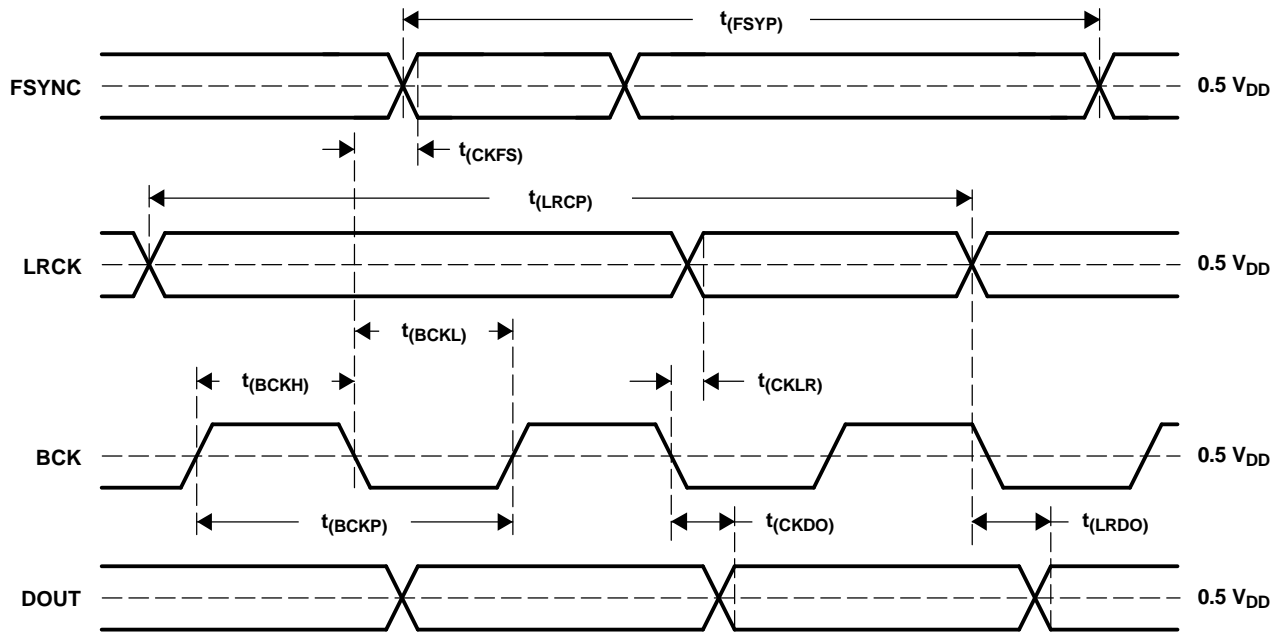


T0017-01

DESCRIPTION	SYMBOL	MIN	TYP	MAX	UNITS
BCK period	$t_{(BCKP)}$	300			ns
BCK pulse duration, HIGH	$t_{(BCKH)}$	120			ns
BCK pulse duration, LOW	$t_{(BCKL)}$	120			ns
LRCK setup time to BCK rising edge	$t_{(LRSU)}$	80			ns
LRCK hold time to BCK rising edge	$t_{(LRHD)}$	40			ns
LRCK period	$t_{(LRCP)}$	20			$\mu$ s
FSYNC setup time to BCK rising edge	$t_{(FSSU)}$	40			ns
FSYNC hold time to BCK rising edge	$t_{(FSHD)}$	40			ns
Delay time, BCK falling edge to DOUT valid	$t_{(CKDO)}$	-20		40	ns
Delay time, LRCK edge to DOUT valid	$t_{(LRDO)}$	-20		40	ns
Rising time of all signals	$t_{(RISE)}$			20	ns
Falling time of all signals	$t_{(FALL)}$			20	ns

NOTE: Timing measurement reference level is  $(V_{IH} + V_{IL})/2$ . Rising and falling time is measured from 10% to 90% of the I/O signal swing. Load capacitance of the DOUT signal is 20 pF.

**Figure 24. Audio Data Interface Timing (Slave Mode: FSYNC, LRCK, and BCK Are Inputs)**



T0018-01

DESCRIPTION	SYMBOL	MIN	TYP	MAX	UNITS
BCK period	$t_{(BCKP)}$	300	$1/64 f_S$	4800	ns
BCK pulse duration, HIGH	$t_{(BCKH)}$	150		2400	ns
BCK pulse duration, LOW	$t_{(BCKL)}$	150		2400	ns
Delay time, BCK falling edge to LRCK valid	$t_{(CKLR)}$	-20		40	ns
LRCK period	$t_{(LRCP)}$	20	$1/f_S$	320	$\mu s$
Delay time, BCK falling edge to FSYNC valid	$t_{(CKFS)}$	-20		40	ns
FSYNC period	$t_{(FSYP)}$	10	$1/2 f_S$	160	$\mu s$
Delay time, BCK falling edge to DOUT valid	$t_{(CKDO)}$	-20		40	ns
Delay time, LRCK edge to DOUT valid	$t_{(LRDO)}$	-20		40	ns
Rising time of all signals	$t_{(RISE)}$			20	ns
Falling time of all signals	$t_{(FALL)}$			20	ns

NOTE: Timing measurement reference level is  $(V_{IH} + V_{IL})/2$ . Rising and falling time is measured from 10% to 90% of the I/O signal swing. Load capacitance of the DOUT signal is 20 pF.

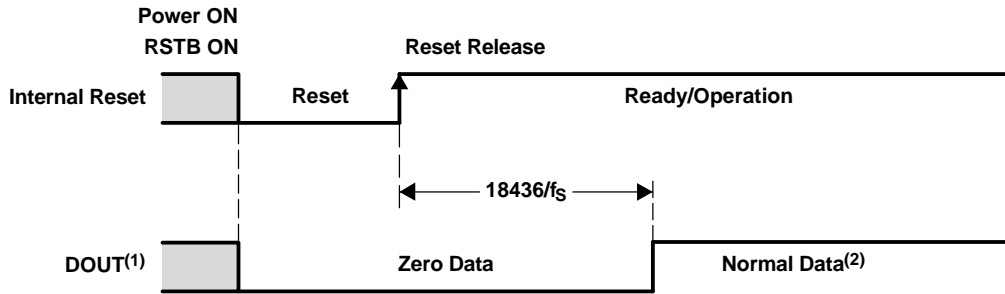
**Figure 25. Audio Data Interface Timing (Master Mode: FSYNC, LRCK, and BCK Are Outputs)**

## SYNCHRONIZATION WITH DIGITAL AUDIO SYSTEM

In slave mode, the PCM1800 operates with LRCK synchronized to the system clock (SYSCLK). The PCM1800 does not require a specific phase relationship between LRCK and SYSCLK, but does require the synchronization of LRCK and SYSCLK. If the relationship between LRCK and SYSCLK changes more than 6 bit clocks (BCK) during one sample period due to LRCK or SYSCLK jitter, internal operation of the ADC halts within  $1/f_S$  and the digital output is forced into the BPZ mode until resynchronization between LRCK and SYSCLK is completed. In case of changes less than 5 bit clocks (BCK), resynchronization does not occur, and the previously described digital output control and discontinuity does not occur.

## ADC DATA OUTPUT AT RESET

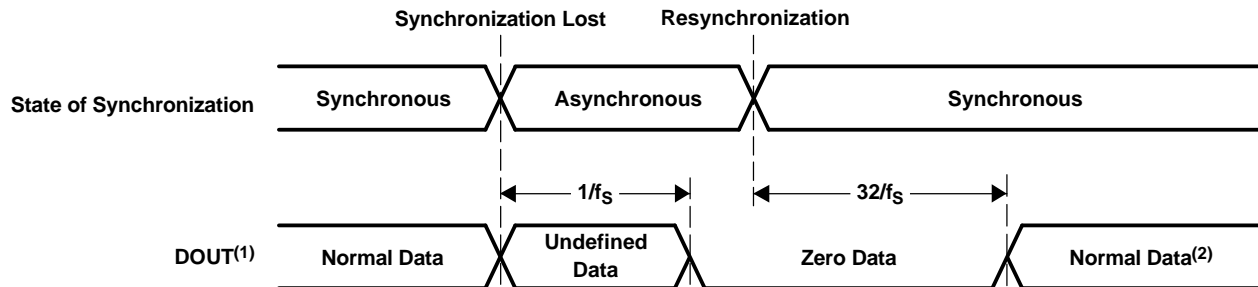
Figure 26 and Figure 27 illustrate the ADC digital output when the reset operation is done and when synchronization is lost, respectively. During undefined data, some noise may be generated in the audio signal. Also, the transition of normal to undefined data and undefined or zero data to normal makes a discontinuity in the data on the digital output, and may generate some noise in the audio signal.



T0019-01

- (1) In the master mode, FSYNC, BCK, and LRCK are outputs similar to DOUT.
- (2) The HPF transient response (exponentially attenuated signal from  $\pm 0.2\%$  dc of FSR with 200-ms time constant) appears initially.

**Figure 26. ADC Digital Output for Power-On Reset and RSTB Control**



T0020-01

- (1) Applies only for slave mode—the loss of synchronization never occurs in master mode.
- (2) The HPF transient response (exponentially attenuated signal from  $\pm 0.2\%$  dc of FSR with 200-ms time constant) appears initially.

**Figure 27. ADC Digital Output During Loss of Synchronization Resynchronization**

### HPF BYPASS CONTROL

The built-in function for dc component rejection can be bypassed by BYPAS (pin 7) control (see Table 4). In bypass mode, the dc component of the input analog signal, the internal dc offset, etc., are also converted and output in the digital output data.

**Table 4. HPF Bypass Control**

BYPAS	HIGH-PASS FILTER (HPF) MODE
Low	Normal (dc cut) mode
High	Bypass (through) mode

## APPLICATION INFORMATION

### BOARD DESIGN AND LAYOUT CONSIDERATIONS

#### $V_{CC}$ , $V_{DD}$ PINS

The digital and analog power supply lines to the PCM1800 should be bypassed to the corresponding ground pins with both 0.1- $\mu$ F ceramic and 10- $\mu$ F tantalum capacitors as close to the pins as possible to maximize the dynamic performance of the ADC. Although the PCM1800 has two power lines to maximize the potential of dynamic performance, using one common power supply is recommended to avoid unexpected power supply problems, such as latch-up or power supply sequence.

#### AGND, DGND PINS

To maximize the dynamic performance of the PCM1800, the analog and digital grounds are not internally connected. These points should have low impedance to avoid digital noise feedback into the analog ground. They should be connected directly to each other under the part to reduce potential noise problems.

#### $V_{IN}$ PINS

A 1- $\mu$ F tantalum capacitor is recommended as an ac-coupling capacitor, which establishes a 5.3-Hz cutoff frequency. If a higher full-scale input voltage is required, the input voltage range can be increased by adding a series resistor to the  $V_{IN}$  pins.

#### $V_{REF}$ INPUTS

A 4.7- $\mu$ F tantalum capacitor is recommended between  $V_{REF1}$ ,  $V_{REF2}$ , and REFCOM to ensure low source impedance for the ADC references. These capacitors should be located as close as possible to the  $V_{REF1}$  and  $V_{REF2}$  pins to reduce dynamic errors on the ADC references. The REFCOM pin also should be connected directly to AGND under the part.

#### $C_{INP}$ and $C_{INN}$ INPUTS

A 470-pF to 1000-pF film capacitor is recommended between  $C_{INPL}$  and  $C_{INNL}$ ,  $C_{INPR}$  and  $C_{INNR}$  to create an antialiasing filter which has a 170-kHz to 80-kHz cutoff frequency. These capacitors should be located as close as possible to the  $C_{INP}$  and  $C_{INN}$  pins to avoid introducing unexpected noise or dynamic errors into the delta-sigma modulator. Four 10-pF–47-pF capacitors between  $C_{INXX}$  and AGND may improve dynamic performance under disadvantageous actual conditions.

#### DOUT, BCK, LRCK, FSYNC PINS

In master mode, the DOUT, BCK, LRCK and FSYNC pins have a large load-drive capability, but locating the buffer near the PCM1800 and minimizing the load capacitance is recommended in order to minimize the digital-analog crosstalk and to maximize dynamic performance potential.

#### SYSTEM CLOCK

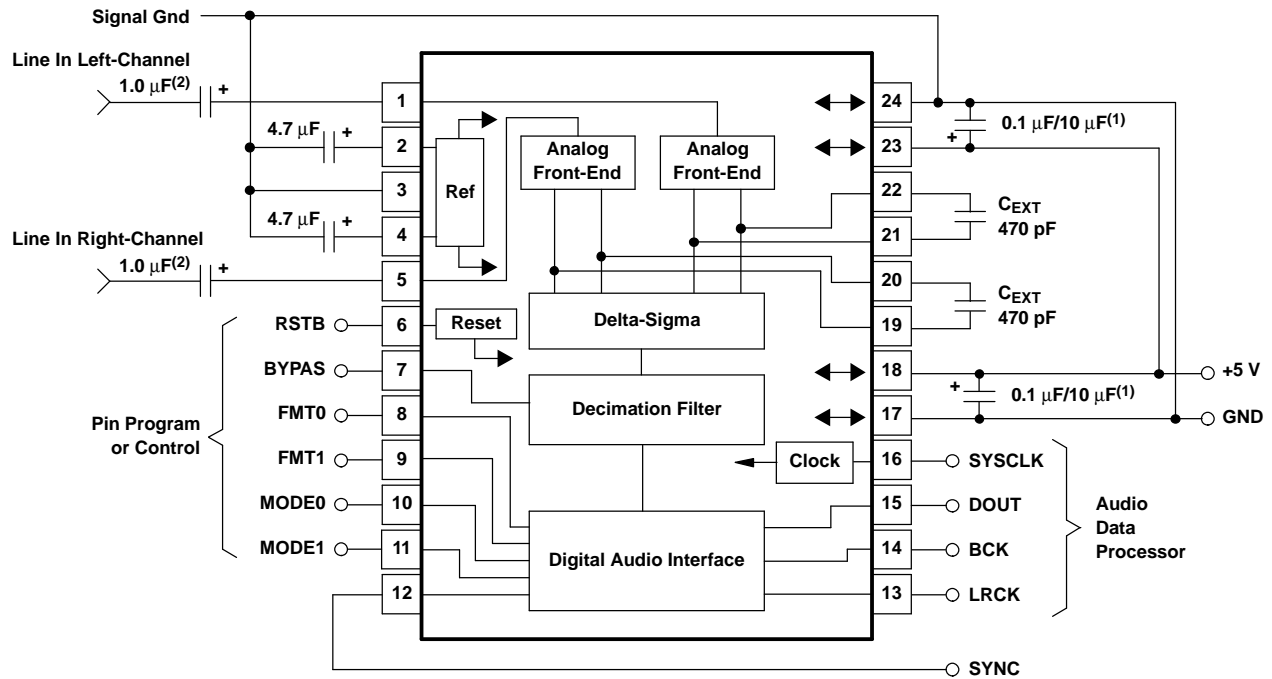
The quality of the system clock can influence dynamic performance in the PCM1800. The duty cycle, jitter, and threshold voltage at the system clock input pin must be carefully managed. When power is supplied to the part, the system clock, bit clock (BCK), and word clock (LRCK) should also be supplied simultaneously. Failure to supply the audio clocks results in a power dissipation increase of up to three times normal dissipation and can degrade long-term reliability if the maximum power dissipation limit is exceeded.

#### RSTB CONTROL

If the capacitance between  $V_{REF1}$  and  $V_{REF2}$  exceeds 4.7  $\mu$ F, an external reset control with a delay-time circuit must be used.

## TYPICAL CIRCUIT CONNECTION DIAGRAM

Figure 28 is a typical circuit connection diagram for which the cutoff frequency of the input HPF is about 5 Hz.



S0012-01

- (1) Bypass capacitor = 0.1- $\mu\text{F}$  ceramic and 10- $\mu\text{F}$  tantalum, depending on layout and power supply.
- (2) A 1- $\mu\text{F}$  capacitor gives a 5.3-Hz cutoff frequency for the input HPF in normal operation and requires a power-on settling period with a 30-ms time constant during power-on initialization.

**Figure 28. Typical Circuit Connection**

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
PCM1800E	ACTIVE	SSOP	DB	24	58	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCM1800E/2K	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCM1800E/2KG4	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCM1800EG4	ACTIVE	SSOP	DB	24	58	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

<b>Products</b>		<b>Applications</b>	
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>	Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>	Automotive	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>	Broadband	<a href="http://www.ti.com/broadband">www.ti.com/broadband</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>	Digital Control	<a href="http://www.ti.com/digitalcontrol">www.ti.com/digitalcontrol</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>	Military	<a href="http://www.ti.com/military">www.ti.com/military</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>	Optical Networking	<a href="http://www.ti.com/opticalnetwork">www.ti.com/opticalnetwork</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>	Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
		Telephony	<a href="http://www.ti.com/telephony">www.ti.com/telephony</a>
		Video & Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>
		Wireless	<a href="http://www.ti.com/wireless">www.ti.com/wireless</a>

Mailing Address: Texas Instruments  
Post Office Box 655303 Dallas, Texas 75265