# TPS784-Q1 300-mA, Low $I_Q$, Low-Dropout Regulator

## 1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1: –40°C to +125°C, $T_A$
- Device junction temperature: –40°C to +150°C, $T_J$
- Input voltage range: 1.65 V to 6.0 V
- Available in fixed-output voltages:
  - Adjustable option: 1.2 V to 5.5 V
  - Fixed options: 0.65 V to 5.0 V
    - 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.0 V, and 3.3 V fixed outputs available
- Output accuracy: 0.75% typical, 1.5% maximum
- Low $I_Q$: 25 µA (typical)
- Ultra-low dropout:
  - 115 mV (max) at 300 mA (3.3 $V_{OUT}$)
- Internal 550 µs soft-start time to reduce inrush current
- Active output discharge:
- Packages:
  - 3-mm × 3-mm wettable flank VSON (8)
  - 5-pin SOT-23

## 2 Applications

- Automotive head units
- Hybrid instrument clusters
- Telematics control units
- DC/DC converters

## 3 Description

The TPS784-Q1 ultra low-dropout regulator (LDO) is a small, low quiescent current LDO that can source 300 mA with excellent line and load transient performance.

The low output noise and great PSRR performance make the device suitable to power sensitive analog loads. The TPS784-Q1 is a flexible device for post regulation because this device supports an input voltage range from 1.65 V to 6.0 V and offers an adjustable output range of 1.2 V to 5.5 V. The device also features fixed output voltages from 0.65 V to 5.0 V for powering common voltage rails.

The TPS784-Q1 offers foldback current limit to reduce power dissipation during over current condition. The EN input helps with power sequencing requirements of the system. The internal soft-start provides a controlled startup reducing the inrush current allowing for lower input capacitance to be used.

The TPS784-Q1 provides an active pulldown circuit to quickly discharge output loads when disabled.

**Device Information**(1)

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| TPS784-Q1 | Wettable flank VSON (8)(2) | 3.00 mm × 3.00 mm |
| | SOT-23 (5) | 2.90 mm × 1.60 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

(2) Preview package.

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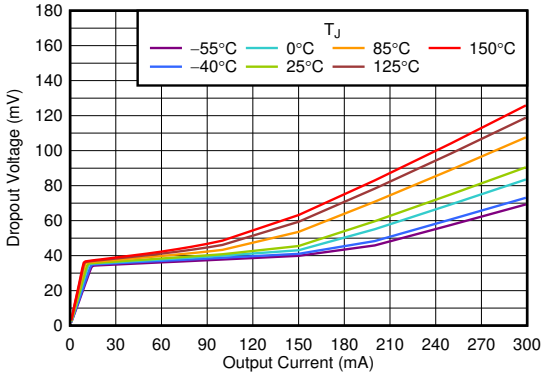
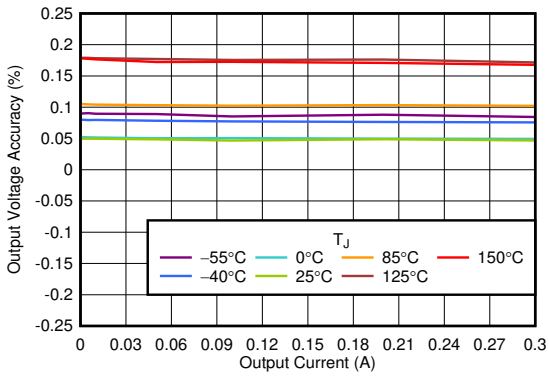
**Dropout vs $I_{OUT}$**




**Output Accuracy vs $I_{OUT}$ for 5.0 V**



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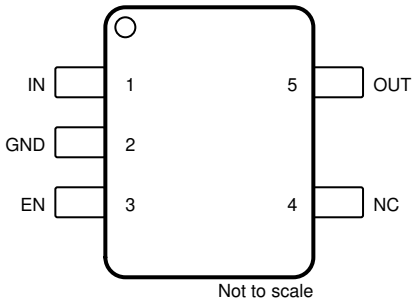
## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

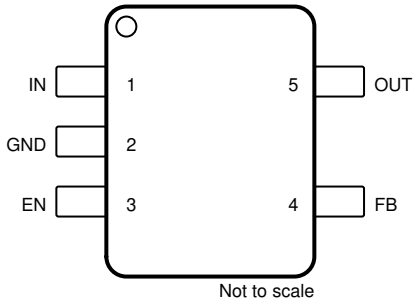
| DATE | REVISION | NOTES |
|---|---|---|
| February 2020 | * | Initial release. |

# 5 Pin Configuration and Functions

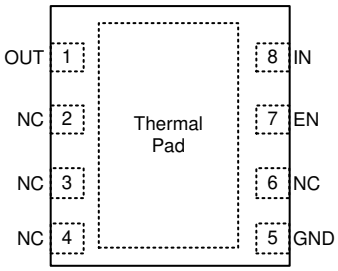
**DBV Package (Fixed)**
**5-Pin SOT-23**
**Top View**



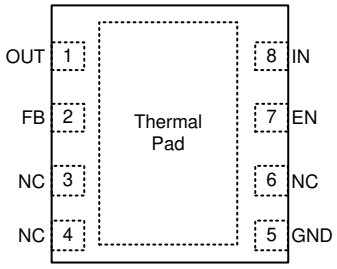

**DBV Package (Adjustable)**
**5-Pin SOT-23**
**Top View**




**DRB Package (Fixed)**
**8-Pin WSON**
**Top View**




**DRB Package (Adjustable)**
**8-Pin WSON**
**Top View**




**Pin Functions:**

| PIN | | | | | I/O | DESCRIPTION |
|---|---|---|---|---|---|---|
| NAME | DBV (Adjustable) | DBV (Fixed) | DRB (Adjustable) | DRB (Fixed) | | |
| EN | 3 | 3 | 7 | 7 | Input | Enable pin. Driving this pin to logic high enables the device; driving this pin to logic low disables the device. |
| FB | 4 | — | 2 | — | Input | This pin is the feedback connection to the center tap of an external resistor divider network that sets the output voltage. This pin must not be left floating. |
| GND | 2 | 2 | 5 | 5 | — | Ground pin. This pin must be connected to ground on the board. |
| IN | 1 | 1 | 8 | 8 | Input | Input pin. For best transient response and to minimize input impedance, use the recommended value or larger ceramic capacitor from IN to ground; see the *Recommended Operating Conditions* table. Place the input capacitor as close to the input of the device as possible. |
| NC | — | 4 | 3, 4, 6 | 2, 3, 4, 6 | — | No internal connection. This pin can be either floated or connected to GND for best thermal performance. |
| OUT | 5 | 5 | 1 | 1 | Output | Regulated output voltage pin. A capacitor is required from OUT to ground for stability. For best transient response, use the nominal recommended value or larger ceramic capacitor from OUT to ground; see the *Recommended Operating Conditions* table and the *Input and Output Capacitor Requirements* section. Place the output capacitor as close to output of the device as possible. |
| Thermal Pad | N/A | N/A | Pad | Pad | — | The thermal pad is electrically connected to the GND pin. Connect the thermal pad to a large-area GND plane for improved thermal performance. |

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# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | MIN | MAX | UNIT |
|---|---|---|---|
| Supply voltage, $V_{IN}$ | –0.3 | 6.5 | V |
| Enable voltage, $V_{EN}$ | –0.3 | 6.5 | V |
| Output voltage, $V_{OUT}$ | –0.3 | $V_{IN}$ + 0.3(2) | V |
| Feedback voltage, $V_{FB}$ | -0.3 | 2 | V |
| Output current, $I_{OUT}$ | Internally limited | | |
| Operating junction temperature, $T_J$ | –40 | 150 | °C |
| Storage temperature, $T_{stg}$ | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The absolute maximum rating is $V_{IN}$ + 0.3 V or 6.5 V, whichever is smaller

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per AEC Q100-002(1) | ±2000 | V |
| | | Charged-device model (CDM), per AEC Q100-011 | ±500 | |

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IN}$ | Input voltage | | 1.65 | | 6.0 | V |
| $V_{OUT}$ | Output voltage | Adjustable output | 1.2 | | 5.5 | V |
| | | Fixed output | 0.65 | | 5.0 | |
| $C_{IN}$ | Input capacitor | | 1 | | | µF |
| $C_{OUT}$ | Output capacitor | | 1(1) | | 200 | µF |
| $I_{OUT}$ | Output current | | 0 | | 300 | mA |
| $C_{OUT,ESR}$ | Output capacitor ESR | | 0.001 | | 1 | Ω |
| $V_{EN}$ | Enable voltage | | 0 | | 6 | V |
| $F_{EN}$ | Enable toggle frequency | | | | 10 | kHz |
| $T_J$ | Junction temperature | | –40 | | 150 | °C |

(1) The minimum effective capacitance is 0.47 µF

## 6.4 Thermal Information

| THERMAL METRIC(1) | | TPS784-Q1 | | UNIT |
|---|---|---|---|---|
| | | DRB (VSON) | DBV (SOT-23) | |
| | | 8 PINS | 5 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 61.8 | 170.8 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 74.1 | 93.1 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 34.3 | 10.2 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 6.2 | 17.5 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 34.1 | 40 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 18.1 | n/a | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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## 6.5 Electrical Characteristics

at operating temperature range ($T_J$ = –40°C to +150°C), $V_{IN}$ = $V_{OUT(NOM)}$ + 0.5 V or 1.65 V (whichever is greater), $I_{OUT}$ = 1 mA, $V_{EN}$ = $V_{IN}$, and $C_{IN}$ = $C_{OUT}$ = 1 µF, unless otherwise noted. All typical values at $T_J$ = 25°C.

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IN}$ | Input voltage | | | 1.65 | | 6.0 | V |
| $V_{OUT}$ | Output voltage | Adjustable output | | 1.2 | | 5.5 | V |
| | | Fixed output | | 0.65 | | 5.0 | |
| | Output accuracy(1) | $T_J$ = 25°C | | –0.75% | | 0.75% | |
| | | $I_{OUT}$ = 1 mA | | –1.5% | | 1.5% | |
| | | 1 mA ≤ $I_{OUT}$ ≤ 300 mA, $V_{OUT(NOM)}$ + 0.5 V ≤ $V_{IN}$ ≤ 6.0 V or 1.65 V (whichever is greater) | –40°C ≤ $T_J$ ≤ 85°C | –0.75% | | 0.75% | |
| | | | –40°C ≤ $T_J$ ≤ 150°C | –1.5% | | 1.5% | |
| | Line regulation | $V_{OUT(NOM)}$ + 0.5 V ≤ $V_{IN}$ ≤ 6.0 V | | | 0.3 | | mV |
| | Load regulation | 1 mA ≤ $I_{OUT}$ ≤ 300 mA | | –15 | | 15 | mV |
| | | 5 mA ≤ $I_{OUT}$ ≤ 300 mA | | –15 | | 15 | |
| $I_{GND}$ | Ground current | $T_J$ = 25°C, $I_{OUT}$ = 0 mA | | 14 | 25 | 31 | µA |
| | | $I_{OUT}$ = 0 mA | | | | 40 | |
| | | $T_J$ = 25°C, $I_{OUT}$ = 300 µA | | | 33 | 45 | |
| | | –40°C ≤ $T_J$ ≤ 85°C , $I_{OUT}$ = 300 µA | | | | 46 | |
| $I_{SHDN}$ | Shutdown current | $V_{EN}$ ≤ 0.3 V, 1.5 V ≤ $V_{IN}$ ≤ 6.0 V, $T_J$ = 25°C | | | 0.15 | 1 | µA |
| | | $V_{EN}$ ≤ 0.3 V, 1.5 V ≤ $V_{IN}$ ≤ 6.0 V, –40°C ≤ $T_J$ ≤ 85°C | | | 0.1 | 1 | |
| | | $V_{EN}$ ≤ 0.3 V, 1.5 V ≤ $V_{IN}$ ≤ 6.0 V, –40°C ≤ $T_J$ ≤ 150°C | | | | 2 | |
| $I_{FB}$ | Feedback pin current (adjustable only) | | | –0.1 | 0.01 | 0.1 | µA |
| $I_{CL}$ | Output current limit | $V_{IN}$ = $V_{OUT(NOM)}$ + 1 V, $V_{OUT}$ = 0.9 x $V_{OUT(NOM)}$(2) | | 320 | | 475 | mA |
| $I_{SC}$ | Short-circuit current limit | $V_{OUT}$ = 0 V | | | 175 | | mA |
| $V_{DO}$ | Dropout voltage | $I_{OUT}$ = 300 mA, $V_{OUT}$ = 0.95 x $V_{OUT(NOM)}$ | 1.2 V ≤ $V_{OUT}$ < 1.5 V | | | 300 | mV |
| | | | 1.5 V ≤ $V_{OUT}$ < 1.8 V | | | 175 | |
| | | | 1.8 V ≤ $V_{OUT}$ < 2.5 V | | | 140 | |
| | | | 2.5 V ≤ $V_{OUT}$ ≤ 5.0 V | | | 115 | |
| $V_{DO}$ | Dropout voltage adjustable output | $I_{OUT}$ = 300 mA, $V_{FB}$ = 1.14 V | 2 V ≤ $V_{IN}$ ≤ 6.0 V | | | 245 | mV |
| PSRR | Power-supply rejection ratio | $I_{OUT}$ = 300 mA, $V_{IN}$ = $V_{OUT}$ + 1 V | f = 1 kHz | | 66 | | dB |
| | | | f = 100 kHz | | 45 | | |
| | | | f = 1 MHz | | 30 | | |
| $V_N$ | Output noise voltage | BW = 10 Hz to 100 kHz, $V_{OUT}$ = 1.2 V | | | 30 | | $µV_{RMS}$ |
| $V_{UVLO,rising}$ | Undervoltage lockout | $V_{IN}$ rising | | 1.32 | 1.42 | 1.58 | V |
| $V_{UVLO,falling}$ | | $V_{IN}$ falling | | 1.17 | 1.29 | 1.42 | V |
| $V_{UVLO,HYST}$ | Undervoltage lockout hysteresis | $V_{IN}$ hysteresis | | | 130 | | mV |
| $t_{STR}$ | Startup time | From EN low-to-high transition to $V_{OUT}$ = $V_{OUT(NOM)}$ x 95%(3) | | | 500 | | µs |
| $V_{HI}$ | EN pin high voltage (enabled) | | | 1.0 | | | V |
| $V_{LO}$ | EN pin low voltage (enabled) | | | | | 0.3 | V |
| $I_{EN}$ | Enable pin current | $V_{IN}$ = $V_{EN}$ = 6.0 V | | | 10 | | nA |
| $R_{PULLDOWN}$ | Pulldown resistance | $V_{IN}$ = 3.3 V | | | 120 | | Ω |
| $T_{SD}$ | Thermal shutdown | Shutdown, temperature increasing | | | 170 | | °C |
| | | Reset, temperature decreasing | | | 155 | | |

(1) Resistor tolerance is not included in overall accuracy in the adjustable version.
(2) The output is being forced to 90% of the nominal $V_{OUT}$ value.
(3) Startup time = time from EN assertion to 0.95×$V_{OUT(NOM)}$.

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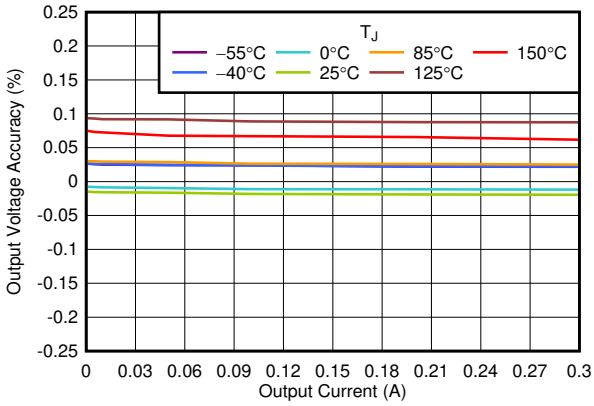
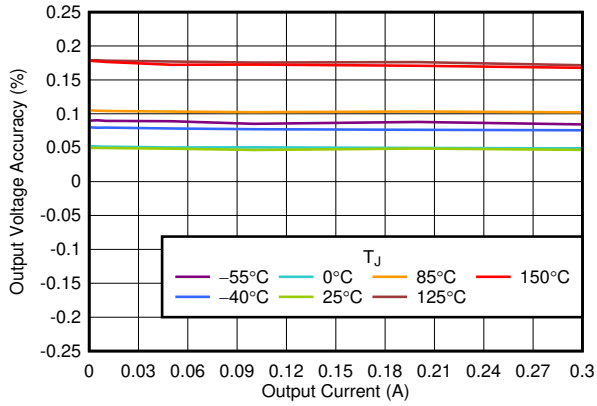
## 6.6 Typical Characteristics

at operating temperature $T_J$ = 25°C, $I_{OUT}$ = 1 mA, $V_{EN}$ = 1.0 V, $C_{IN}$ = 1.0 µF, $C_{OUT}$ = 1.0 µF, and $V_{IN}$ = $V_{OUT(NOM)}$ + 0.5 V or 1.65 V (whichever is greater), unless otherwise noted; typical values are at $T_J$ = 25°C



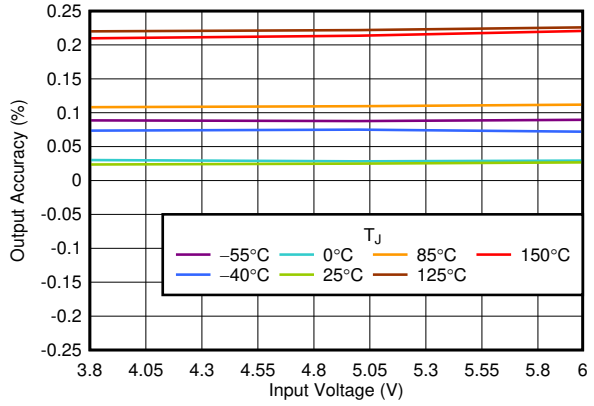

$V_{OUT}$ = 1.2 V

**Figure 1. Output Accuracy vs $I_{OUT}$**



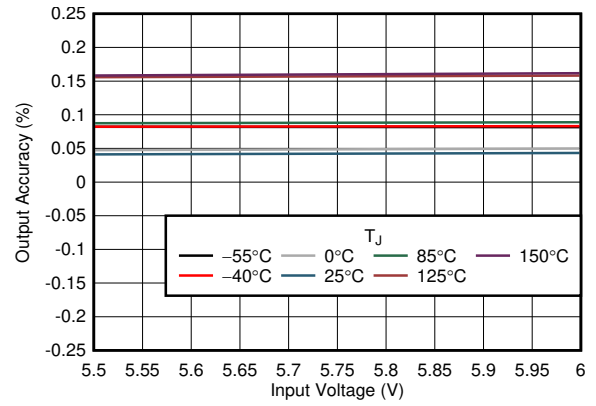

$V_{OUT}$ = 5.0 V

**Figure 2. Output Accuracy vs $I_{OUT}$**



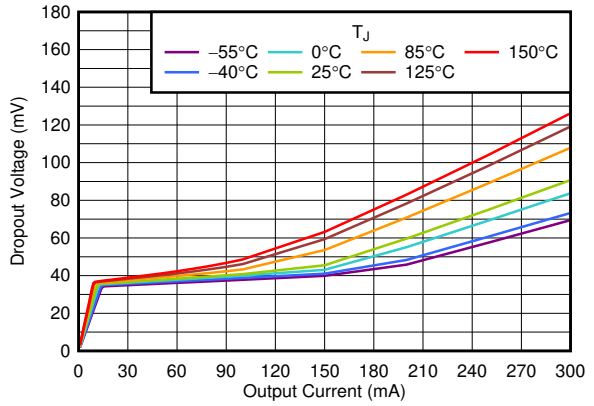

$V_{OUT}$ = 3.3 V

**Figure 3. Output Accuracy vs $V_{IN}$**



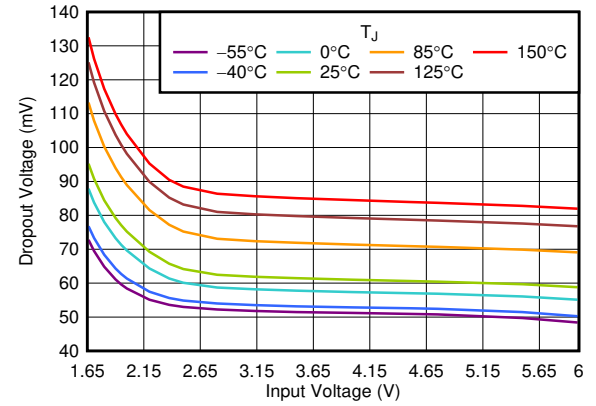

$V_{OUT}$ = 5.0 V

**Figure 4. Output Accuracy vs $V_{IN}$**




$V_{OUT}$ = 1.2 V

**Figure 5. Dropout Voltage vs $I_{OUT}$**




$V_{OUT}$ = 1.2 V

**Figure 6. Dropout Voltage vs $V_{IN}$**

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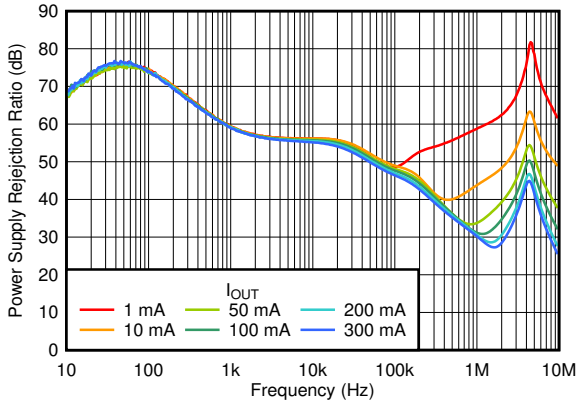
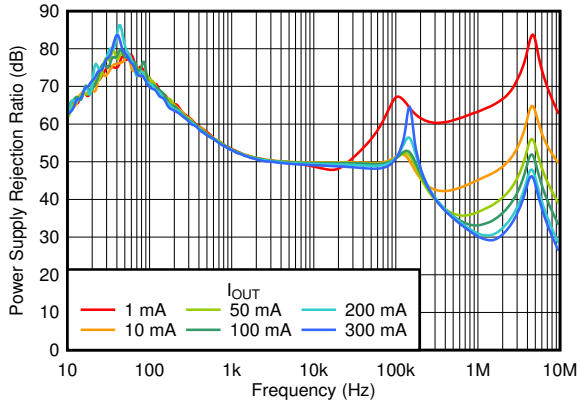
## Typical Characteristics (continued)

at operating temperature $T_J$ = 25°C, $I_{OUT}$ = 1 mA, $V_{EN}$ = 1.0 V, $C_{IN}$ = 1.0 µF, $C_{OUT}$ = 1.0 µF, and $V_{IN}$ = $V_{OUT(NOM)}$ + 0.5 V or 1.65 V (whichever is greater), unless otherwise noted; typical values are at $T_J$ = 25°C



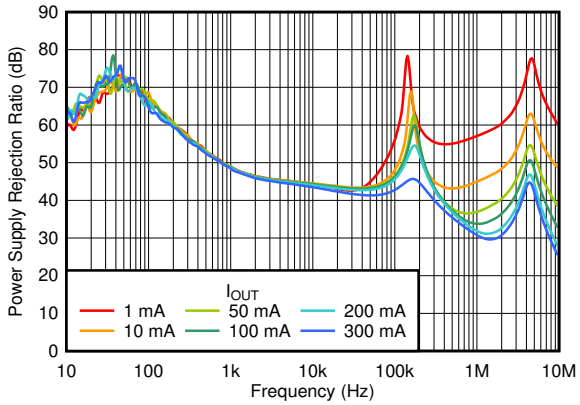

$V_{IN}$ = 2.2 V, $C_{IN}$ = 0 µF, $V_{OUT}$ = 1.2 V

**Figure 7. PSRR vs Frequency and $I_{OUT}$**



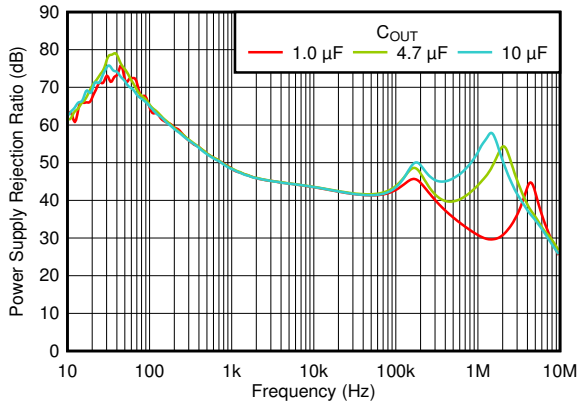

$V_{IN}$ = 4.3 V, $C_{IN}$ = 0 µF, $V_{OUT}$ = 3.3 V

**Figure 8. PSRR vs Frequency and $I_{OUT}$**



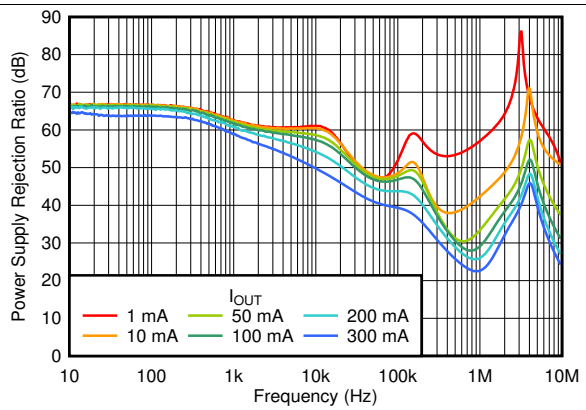

$V_{IN}$ = 6 V, $C_{IN}$ = 0 µF, $V_{OUT}$ = 5.0 V

**Figure 9. PSRR vs Frequency and $I_{OUT}$**



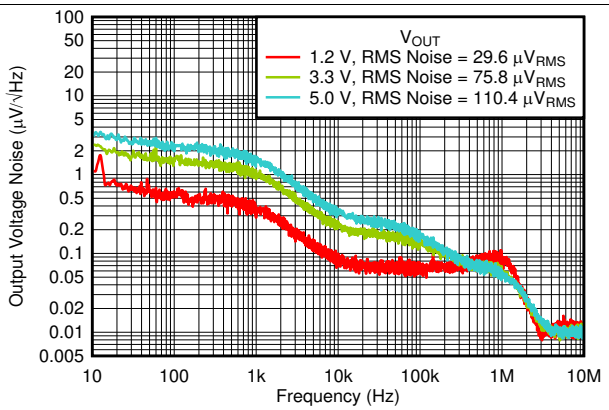

$V_{IN}$ = 6 V, $C_{IN}$ = 0 µF, $V_{OUT}$ = 5.0 V, $I_{OUT}$ = 300 mA

**Figure 10. PSRR vs Frequency and $C_{OUT}$**




$V_{IN}$ = 1.65 V, $C_{IN}$ = 0 µF, $V_{OUT}$ = 0.65 V

**Figure 11. PSRR vs Frequency and $I_{OUT}$**




$V_{IN}$ = $V_{OUT(nom)}$ + 1 V, $I_{OUT}$ = 300 mA,
$V_{RMS}$ BW = 10 Hz to 100 kHz

**Figure 12. Output Noise vs Frequency and $V_{OUT}$**

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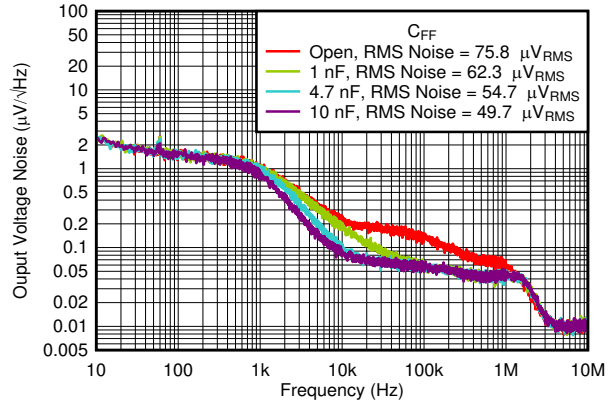
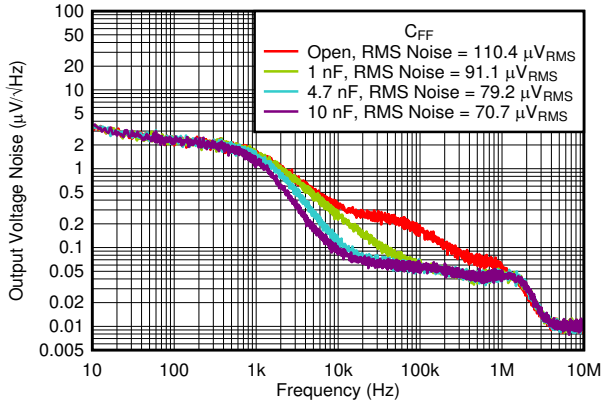
## Typical Characteristics (continued)

at operating temperature $T_J$ = 25°C, $I_{OUT}$ = 1 mA, $V_{EN}$ = 1.0 V, $C_{IN}$ = 1.0 µF, $C_{OUT}$ = 1.0 µF, and $V_{IN}$ = $V_{OUT(NOM)}$ + 0.5 V or 1.65 V (whichever is greater), unless otherwise noted; typical values are at $T_J$ = 25°C



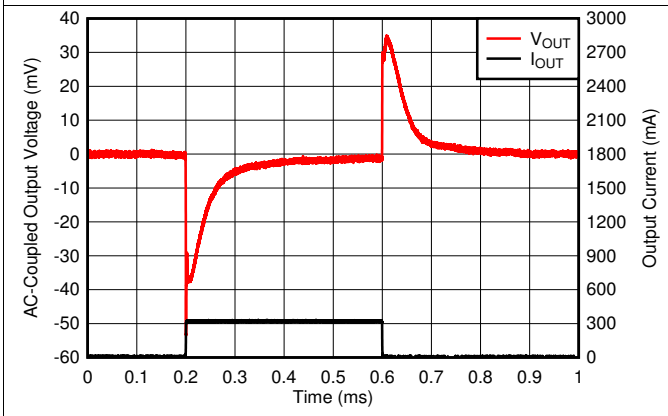

$V_{IN}$ = 4.3 V, $V_{OUT}$ = 3.3 V, $I_{OUT}$ = 300 mA,
$V_{RMS}$ BW = 10 Hz to 100 kHz

**Figure 13. Output Noise vs Frequency and $C_{FF}$**



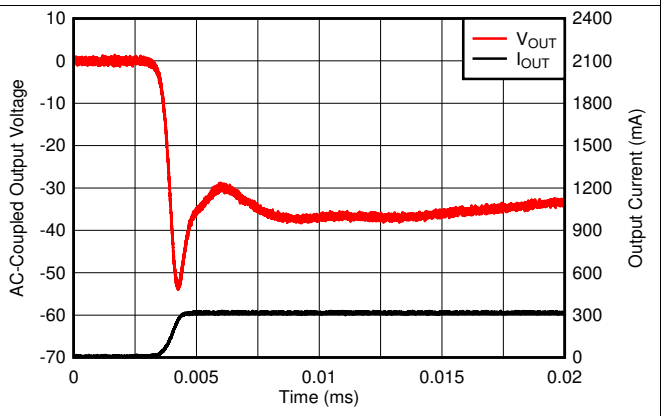

$V_{IN}$ = 6 V, $V_{OUT}$ = 5.0 V, $I_{OUT}$ = 300 mA,
$V_{RMS}$ BW = 10 Hz to 100 kHz

**Figure 14. Output Noise vs Frequency and $C_{FF}$**



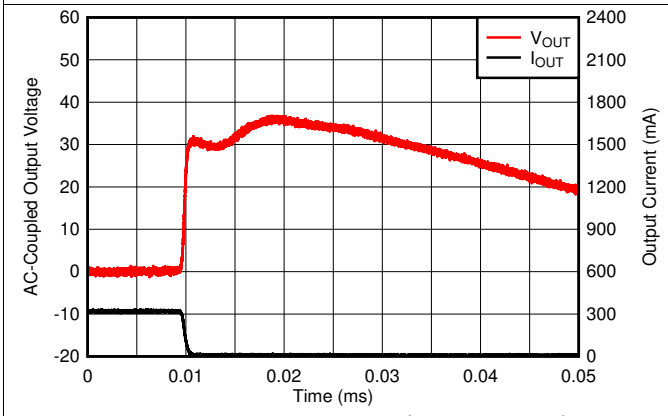

$V_{IN}$ = 5.5 V, $V_{OUT}$ = 5.0 V, $I_{OUT}$ slew rate = 0.5 A/µs

**Figure 15. $I_{OUT}$ Transient From 1 mA to 300 mA**



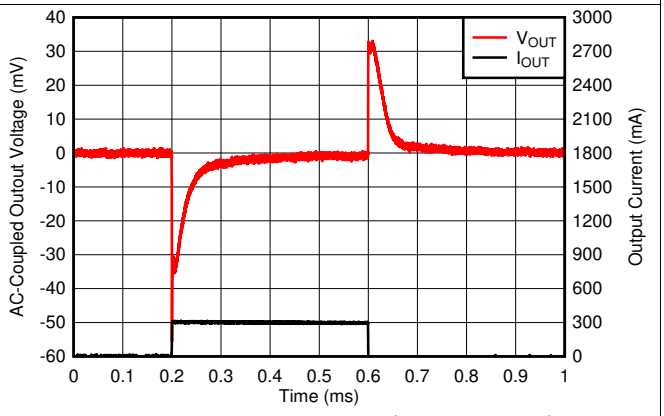

$V_{IN}$ = 5.5 V, $V_{OUT}$ = 5.0 V, $I_{OUT}$ slew rate = 0.5 A/µs

**Figure 16. $I_{OUT}$ Transient From 1 mA to 300 mA**




$V_{IN}$ = 5.5 V, $V_{OUT}$ = 5.0 V, $I_{OUT}$ slew rate = 0.5 A/µs

**Figure 17. $I_{OUT}$ Transient From 300 mA to 1 mA**



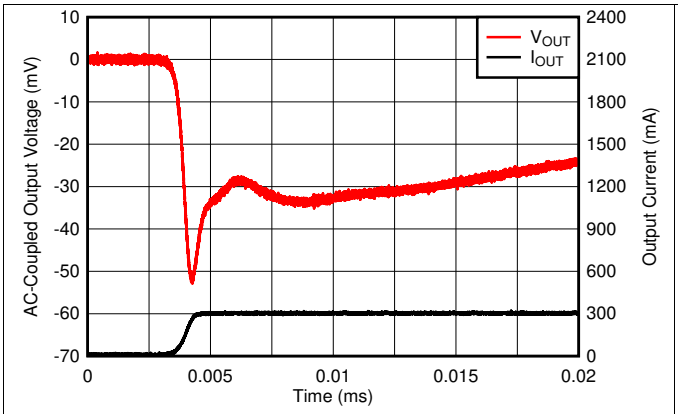

$V_{IN}$ = 3.8 V, $V_{OUT}$ = 3.3 V, $I_{OUT}$ slew rate = 0.5 A/µs

**Figure 18. $I_{OUT}$ Transient From 1 mA to 300 mA**

ADVANCE INFORMATION

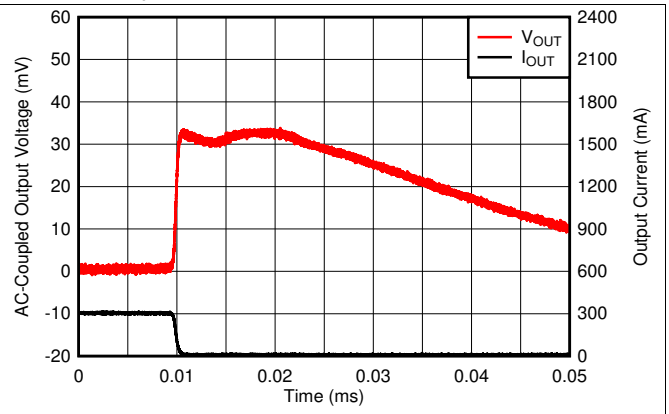
## Typical Characteristics (continued)

at operating temperature $T_J$ = 25°C, $I_{OUT}$ = 1 mA, $V_{EN}$ = 1.0 V, $C_{IN}$ = 1.0 µF, $C_{OUT}$ = 1.0 µF, and $V_{IN}$ = $V_{OUT(NOM)}$ + 0.5 V or 1.65 V (whichever is greater), unless otherwise noted; typical values are at $T_J$ = 25°C



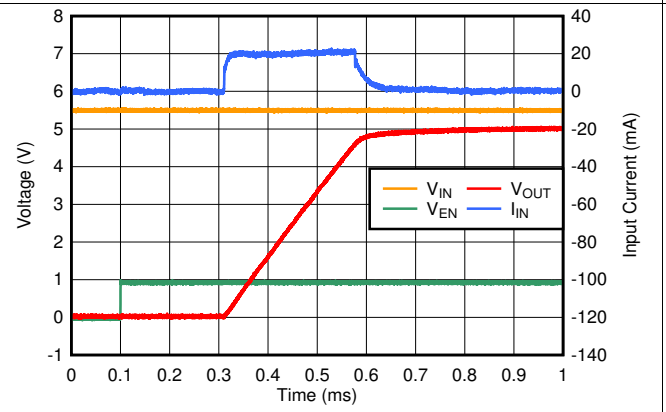

$V_{IN}$ = 3.8 V, $V_{OUT}$ = 3.3 V, $I_{OUT}$ slew rate = 0.5 A/µs

**Figure 19. $I_{OUT}$ Transient From 1-mA to 300-mA Rising Edge**



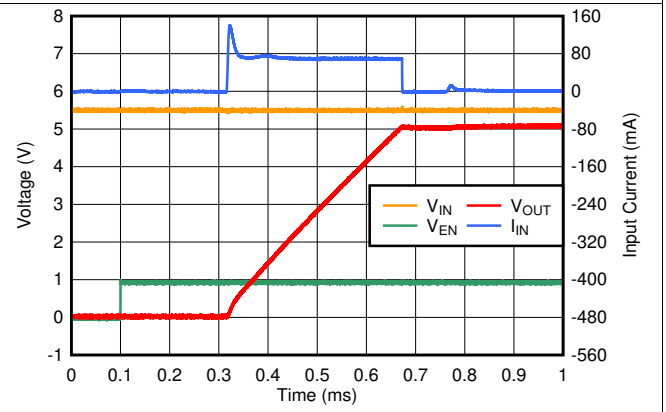

$V_{IN}$ = 3.8 V, $V_{OUT}$ = 3.3 V, $I_{OUT}$ slew rate = 0.5 A/µs

**Figure 20. $I_{OUT}$ Transient From 1-mA to 300-mA Falling Edge**




$V_{IN}$ = 5.5 V, $C_{IN}$ = 0 µF, $V_{OUT}$ = 5.0 V, $I_{OUT}$ = 0 mA

**Figure 21. Startup Inrush Current With $C_{OUT}$ = 1 µF**




$V_{IN}$ = 5.5 V, $C_{IN}$ = 0 µF, $V_{OUT}$ = 5.0 V, $I_{OUT}$ = 0 mA

**Figure 22. Startup Inrush Current With $C_{OUT}$ = 4.7 µF**

ADVANCE INFORMATION

# 7 Detailed Description

## 7.1 Overview

The TPS784-Q1 is an ultra low-dropout, high PSRR, high-accuracy linear voltage regulator that is optimized for excellent transient performance. These characteristics make the device ideal for most automotive applications.

This regulator offers active discharge, foldback current limit, shutdown, and thermal protection.

## 7.2 Functional Block Diagrams

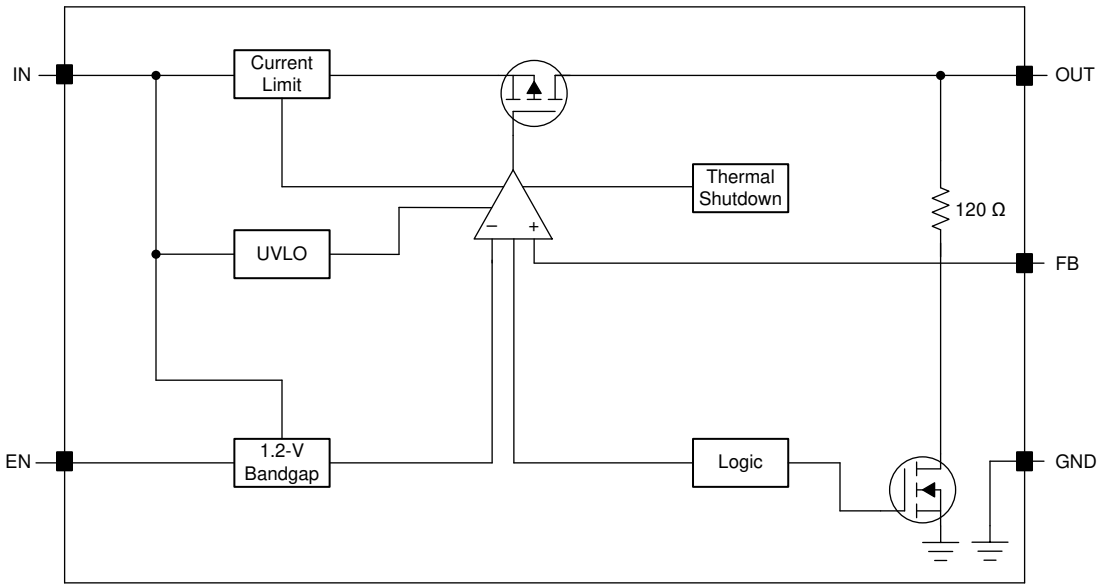



**Figure 23. Adjustable-Version Block Diagram**

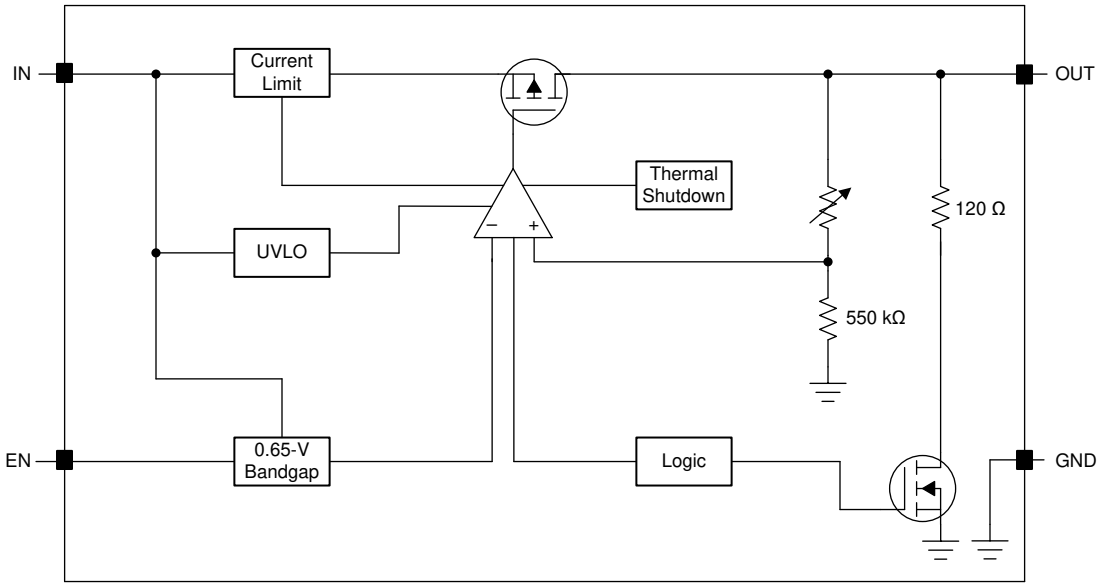



**Figure 24. Fixed-Version Block Diagram**

ADVANCE INFORMATION

## 7.3 Feature Description

### 7.3.1 Active Discharge

The device has an internal pulldown MOSFET that connects an $R_{PULLDOWN}$ resistor to ground when the device is disabled to actively discharge the output voltage. The active discharge circuit is activated by the enable pin.

Do not rely on the active discharge circuit for discharging a large amount of output capacitance after the input supply has collapsed because reverse current can possibly flow from the output to the input. This reverse current flow can cause damage to the device. Limit reverse current to no more than 5% of the device rated current for a short period of time.

### 7.3.2 Foldback Current Limit

The device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a hybrid brickwall-foldback scheme. The current limit transitions from a brickwall scheme to a foldback scheme at the foldback voltage ($V_{FOLDBACK}$). In a high-load current fault with the output voltage above $V_{FOLDBACK}$, the brickwall scheme limits the output current to the current limit ($I_{CL}$). When the voltage drops below $V_{FOLDBACK}$, a foldback current limit activates that scales back the current as the output voltage approaches GND. When the output is shorted, the device supplies a typical current called the short-circuit current limit ($I_{SC}$). $I_{CL}$ and $I_{SC}$ are listed in the *Electrical Characteristics* table.

For this device, $V_{FOLDBACK} = 0.4\ V \times V_{OUT(NOM)}$.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brickwall current limit, the pass transistor dissipates power [$(V_{IN} – V_{OUT}) \times I_{CL}$]. When the device output is shorted and the output is below $V_{FOLDBACK}$, the pass transistor dissipates power [$(V_{IN} – V_{OUT}) \times I_{SC}$]. If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition continues, the device cycles between current limit and thermal shutdown. For more information on current limits, see the *Know Your Limits* application report.

Figure 25 shows a diagram of the foldback current limit.

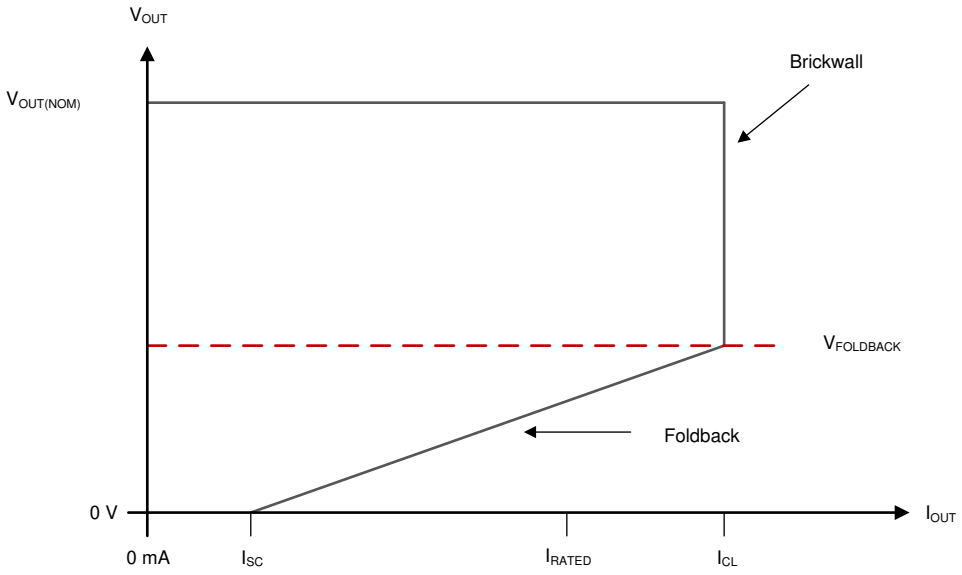



**Figure 25. Foldback Current Limit**

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## Feature Description (continued)

### 7.3.3 Shutdown

The enable pin (EN) is active high. Enable the device by forcing the voltage of the enable pin to exceed the minimum EN pin high-level input voltage (see the *Electrical Characteristics* table). Turn off the device by forcing the voltage of the enable pin to drop below the maximum EN pin low-level input voltage (see the *Electrical Characteristics* table). If shutdown capability is not required, connect EN to IN.

This device has an internal pulldown circuit that activates when the device is disabled to actively discharge the output voltage.

### 7.3.4 Dropout Voltage

Dropout voltage ($V_{DO}$) is defined as the input voltage minus the output voltage ($V_{IN} – V_{OUT}$) at the rated output current ($I_{RATED}$), where the pass transistor is fully on. $I_{RATED}$ is the maximum $I_{OUT}$ listed in the *Recommended Operating Conditions* table. The pass transistor is in the ohmic or triode region of operation, and acts as a switch. The dropout voltage indirectly specifies a minimum input voltage greater than the nominal programmed output voltage at which the output voltage is expected to stay in regulation. If the input voltage falls to less than the nominal output regulation, then the output voltage falls as well.

For a CMOS regulator, the dropout voltage is determined by the drain-source on-state resistance ($R_{DS(ON)}$) of the pass transistor. Therefore, if the linear regulator operates at less than the rated current, the dropout voltage for that current scales accordingly. Use Equation 1 to calculate the $R_{DS(ON)}$ of the device.

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \quad (1)$$

### 7.3.5 Undervoltage Lockout (UVLO)

The device has an independent undervoltage lockout (UVLO) circuit that monitors the input voltage, allowing a controlled and consistent turn on and off of the output voltage. To prevent the device from turning off if the input drops during turn on, the UVLO has hysteresis as specified in the *Electrical Characteristics* table.

### 7.3.6 Thermal Shutdown

The device contains a thermal shutdown protection circuit to disable the device when the junction temperature ($T_J$) of the pass transistor rises to $T_{SD(shutdown)}$ (typical). Thermal shutdown hysteresis assures that the device resets (turns on) when the temperature falls to $T_{SD(reset)}$ (typical).

The thermal time-constant of the semiconductor die is fairly short, thus the device may cycle on and off when thermal shutdown is reached until power dissipation is reduced. Power dissipation during startup can be high from large $V_{IN} – V_{OUT}$ voltage drops across the device or from high inrush currents charging large output capacitors. Under some conditions, the thermal shutdown protection disables the device before startup completes.

For reliable operation, limit the junction temperature to the maximum listed in the *Recommended Operating Conditions* table. Operation above this maximum temperature causes the device to exceed its operational specifications. Although the internal protection circuitry of the device is designed to protect against thermal overall conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown or above the maximum recommended junction temperature reduces long-term reliability.

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## 7.4 Device Functional Modes

### 7.4.1 Device Functional Mode Comparison

The *Device Functional Mode Comparison* table shows the conditions that lead to the different modes of operation. See the *Electrical Characteristics* table for parameter values.

**Table 1. Device Functional Mode Comparison**

| OPERATING MODE | PARAMETER | | | |
|---|---|---|---|---|
| | $V_{IN}$ | $V_{EN}$ | $I_{OUT}$ | $T_J$ |
| Normal operation | $V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$ | $V_{EN} > V_{EN(HI)}$ | $I_{OUT} < I_{OUT(max)}$ | $T_J < T_{SD(shutdown)}$ |
| Dropout operation | $V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$ | $V_{EN} > V_{EN(HI)}$ | $I_{OUT} < I_{OUT(max)}$ | $T_J < T_{SD(shutdown)}$ |
| Disabled (any true condition disables the device) | $V_{IN} < V_{UVLO}$ | $V_{EN} < V_{EN(LOW)}$ | Not applicable | $T_J > T_{SD(shutdown)}$ |

### 7.4.2 Normal Operation

The device regulates to the nominal output voltage when the following conditions are met:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The output current is less than the current limit ($I_{OUT} < I_{CL}$)
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD}$)
- The enable voltage has previously exceeded the enable rising threshold voltage and has not yet decreased to less than the enable falling threshold

### 7.4.3 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass transistor is in the ohmic or triode region, and acts as a switch. Line or load transients in dropout can result in large output-voltage deviations.

When the device is in a steady dropout state (defined as when the device is in dropout, $V_{IN} < V_{OUT(NOM)} + V_{DO}$, directly after being in a normal regulation state, but *not* during startup), the pass transistor is driven into the ohmic or triode region. When the input voltage returns to a value greater than or equal to the nominal output voltage plus the dropout voltage ($V_{OUT(NOM)} + V_{DO}$), the output voltage can overshoot for a short period of time while the device pulls the pass transistor back into the linear region.

### 7.4.4 Disabled

The output of the device can be shutdown by forcing the voltage of the enable pin to less than the maximum EN pin low-level input voltage (see the *Electrical Characteristics* table). When disabled, the pass transistor is turned off, internal circuits are shutdown, and the output voltage is actively discharged to ground by an internal discharge circuit from the output to ground.

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# 8 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

### 8.1.1 Adjustable Device Feedback Resistors

The adjustable-version device requires external feedback divider resistors to set the output voltage. Figure 26 shows how the output voltage can be configured from 1.2 V to 5.5 V by using a resistor divider network.

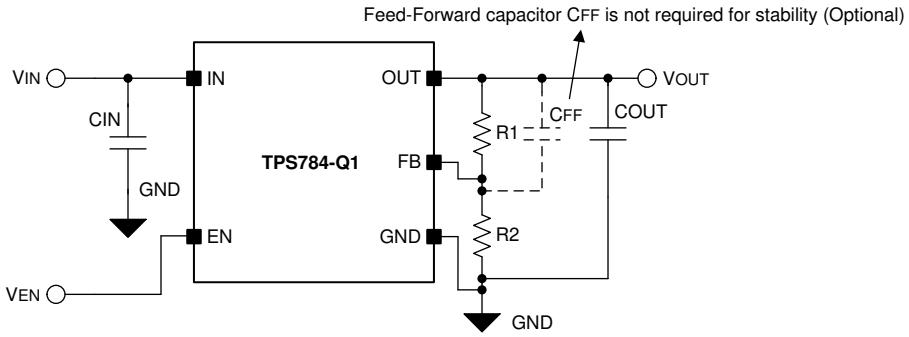


**Figure 26. Adjustable Operation**

Equation 2 calculates how the $R_1$ and $R_2$ resistors are used to set the output voltage:

$$V_{OUT} = V_{FB} \times (1 + R_1 / R_2) + I_{FB} \times R_2 \quad (2)$$

To disregard the effect of the FB pin current error term in Equation 2 and to achieve best accuracy, keep $R_2$ smaller than 80 kΩ to ensure the current flowing through $R_2$ is at least 100 times larger than the $I_{FB}$ current listed in the *Electrical Characteristics* table. Lowering the value of $R_2$ increases the immunity against noise injection. Increasing the value of $R_2$ reduces the quiescent current for achieving higher efficiency at low load currents. Equation 3 calculates the setting that provides the maximum feedback divider series resistance.

$$(R_1 + R_2) \leq V_{OUT} / (I_{FB} \times 100) \quad (3)$$

### 8.1.2 Recommended Capacitor Types

The device is designed to be stable using low equivalent series resistance (ESR) ceramic capacitors at the input and output. Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended, but must be used with good judgment. Ceramic capacitors that employ X7R-, X5R-, and C0G-rated dielectric materials provide relatively good capacitive stability across temperature, whereas the use of Y5V-rated capacitors is discouraged because of large variations in capacitance.

Regardless of the ceramic capacitor type selected, the effective capacitance varies with operating voltage and temperature. As a rule of thumb, expect the effective capacitance to decrease by as much as 50%. The input and output capacitors recommended in the *Recommended Operating Conditions* table account for an effective capacitance of approximately 50% of the nominal value.

### 8.1.3 Input and Output Capacitor Requirements

The device requires an input capacitor of 1.0 µF or larger as specified in the *Recommended Operating Conditions* table for stability. A higher value capacitor may be necessary if large, fast rise-time load or line transients are anticipated or if the device is located several inches from the input power source.

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## Application Information (continued)

The device also requires an output capacitor of 1.0 µF or larger as specified in the *Recommended Operating Conditions* table for stability. Dynamic performance of the device is improved by using a higher capacitor than the minimum output capacitor.

### 8.1.4 Dropout Voltage

The device uses a PMOS pass transistor to achieve low dropout. When ($V_{IN}$ – $V_{OUT}$) is less than the dropout voltage ($V_{DO}$), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. $V_{DO}$ scales approximately with output current because the PMOS device behaves like a resistor in dropout mode. As with any linear regulator, PSRR and transient response degrade as ($V_{IN}$ – $V_{OUT}$) approaches dropout operation.

### 8.1.5 Exiting Dropout

Some applications have transients that place the LDO into dropout, such as slower ramps on $V_{IN}$ during start-up. As with other LDOs, the output can overshoot on recovery from these conditions. A ramping input supply causes an LDO to overshoot on start-up, as shown in Figure 27, when the slew rate and voltage levels are in the correct range. Use an enable signal to avoid this condition.

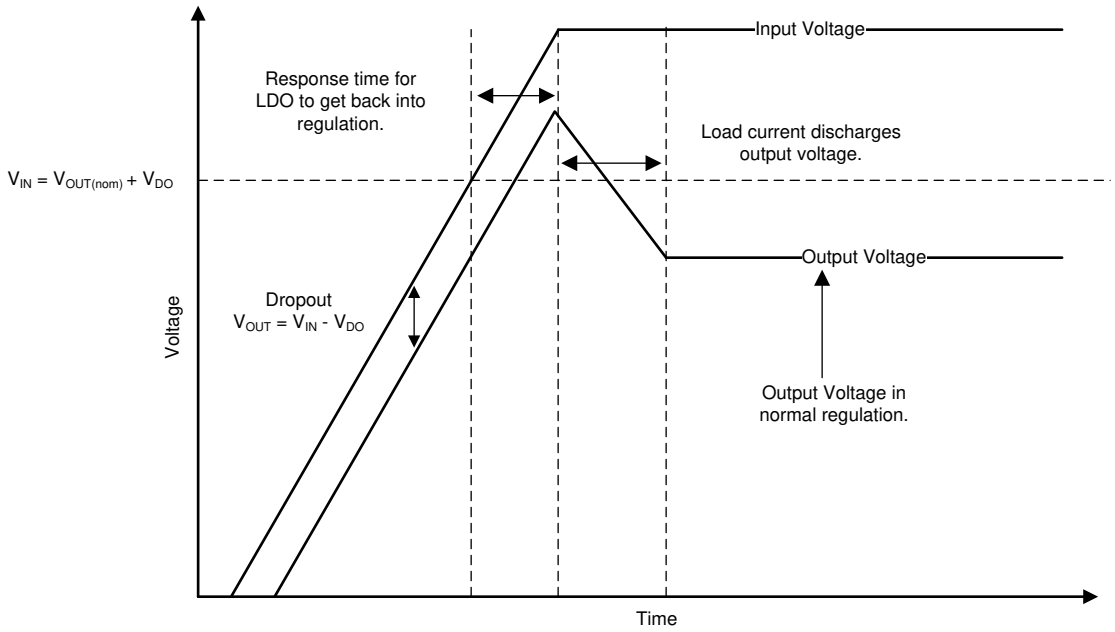


**Figure 27. Start-Up Into Dropout**

Line transients out of dropout can also cause overshoot on the output of the regulator. These overshoots are caused by the error amplifier having to drive the gate capacitance of the pass element and bring the gate back to the correct voltage for proper regulation. Figure 28 illustrates what is happening internally with the gate voltage and how overshoot can be caused during operation. When the LDO is placed in dropout, the gate voltage ($V_{GS}$) is pulled all the way down to ground to give the pass device the lowest on-resistance as possible. However, if a line transient occurs when the device is in dropout, the loop is not in regulation and can cause the output to overshoot until the loop responds and the output current pulls the output voltage back down into regulation. If these transients are not acceptable, then continue to add input capacitance in the system until the transient is slow enough to reduce the overshoot.

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## Application Information (continued)

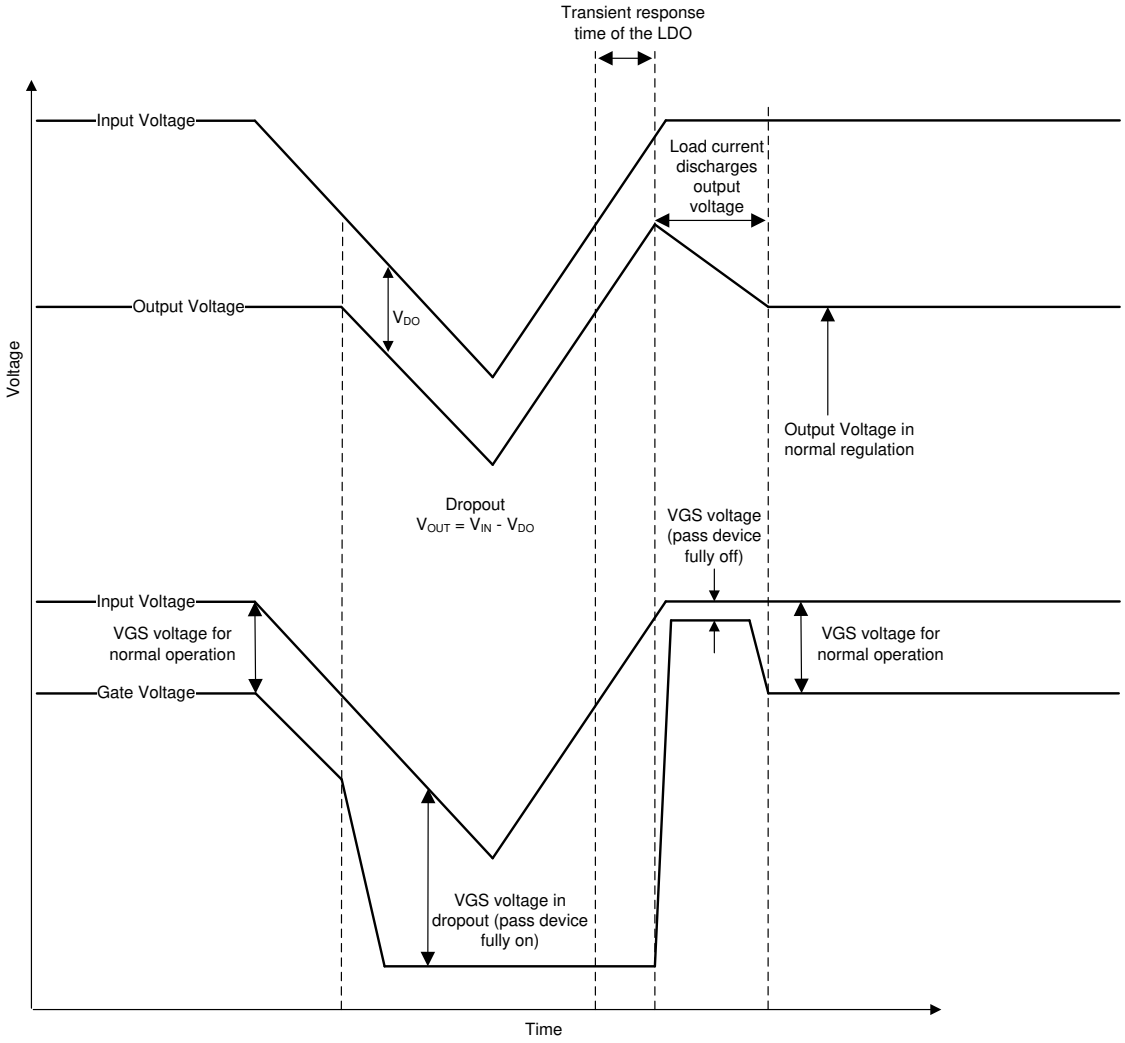


**Figure 28. Line Transients From Dropout**

### 8.1.6 Reverse Current

As with most LDOs, excessive reverse current can damage this device.

Reverse current flows through the body diode on the pass element instead of the normal conducting channel. At high magnitudes, this current flow degrades the long-term reliability of the device, as a result of one of the following conditions:

- Degradation caused by electromigration
- Excessive heat dissipation
- Potential for a latch-up condition

Conditions where reverse current can occur are outlined in this section, all of which can exceed the absolute maximum rating of $V_{OUT} > V_{IN} + 0.3$ V:

- If the device has a large $C_{OUT}$ and the input supply collapses with little or no load current
- The output is biased when the input supply is not established
- The output is biased above the input supply

ADVANCE INFORMATION

## Application Information (continued)

If reverse current flow is expected in the application, external protection must be used to protect the device. Figure 29 shows one approach of protecting the device.

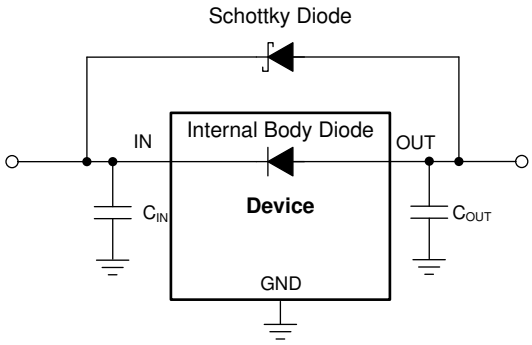


**Figure 29. Example Circuit for Reverse Current Protection Using a Schottky Diode**

### 8.1.7 Feed-Forward Capacitor ($C_{FF}$)

For the adjustable-voltage version device, a feed-forward capacitor ($C_{FF}$) can be connected from the OUT pin to the FB pin. $C_{FF}$ improves transient, noise, and PSRR performance, but is not required for regulator stability. Recommended $C_{FF}$ values are listed in the *Recommended Operating Conditions* table. A higher capacitance $C_{FF}$ can be used; however, the startup time increases. For a detailed description of $C_{FF}$ tradeoffs, see the *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator* application report.

### 8.1.8 Power Dissipation ($P_D$)

Circuit reliability demands that proper consideration be given to device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must be as free as possible of other heat-generating devices that cause added thermal stresses.

As a first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. Use Equation 4 to approximate $P_D$:

$$P_D = (V_{IN} – V_{OUT}) \times I_{OUT} \quad (4)$$

Power dissipation can be minimized, and thus greater efficiency achieved, by proper selection of the system voltage rails. Proper selection allows the minimum input-to-output voltage differential to be obtained. The low dropout of the TPS784-Q1 allows for maximum efficiency across a wide range of output voltages.

The main heat conduction path for the device is through the thermal pad on the package. As such, the thermal pad must be soldered to a copper pad area under the device. This pad area contains an array of plated vias that conduct heat to any inner plane areas or to a bottom-side copper plane.

The maximum power dissipation determines the maximum allowable junction temperature ($T_J$) for the device. According to Equation 5, power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air ($T_A$). Equation 6 rearranges Equation 5 for output current.

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad (5)$$

$$I_{OUT} = (T_J – T_A) / [R_{\theta JA} \times (V_{IN} – V_{OUT})] \quad (6)$$

Unfortunately, this thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The $R_{\theta JA}$ recorded in the *Recommended Operating Conditions* table is determined by the JEDEC standard, PCB, and copper-spreading area, and is only used as a relative measure of package thermal performance. For a well-designed thermal layout, $R_{\theta JA}$ is actually the sum of the X2SON package junction-to-case (bottom) thermal resistance ($R_{\theta JC(bot)}$) plus the thermal resistance contribution by the PCB copper.

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## Application Information (continued)

### 8.1.8.1 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi ($\Psi$) thermal metrics to estimate the junction temperatures of the LDO when in-circuit on a typical PCB board application. These metrics are not strictly speaking thermal resistances, but rather offer practical and relative means of estimating junction temperatures. These psi metrics are determined to be significantly independent of the copper-spreading area. The key thermal metrics ($\Psi_{JT}$ and $\Psi_{JB}$) are used in accordance with Equation 7 and are given in the *Recommended Operating Conditions* table.

$$\Psi_{JT} : T_J = T_T + \Psi_{JT} \times P_D \text{ and } \Psi_{JB} : T_J = T_B + \Psi_{JB} \times P_D \quad (7)$$

where:

- $P_D$ is the power dissipated as explained in Equation 4
- $T_T$ is the temperature at the center-top of the device package, and
- $T_B$ is the PCB surface temperature measured 1 mm from the device package and centered on the package edge

### 8.1.8.2 Recommended Area for Continuous Operation

The operational area of an LDO is limited by the dropout voltage, output current, junction temperature, and input voltage. The recommended area for continuous operation for a linear regulator is given in Figure 30 and can be separated into the following parts:

- Dropout voltage limits the minimum differential voltage between the input and the output ($V_{IN} – V_{OUT}$) at a given output current level. See the *Dropout Operation* section for more details.
- The rated output currents limits the maximum recommended output current level. Exceeding this rating causes the device to fall out of specification.
- The rated junction temperature limits the maximum junction temperature of the device. Exceeding this rating causes the device to fall out of specification and reduces long-term reliability.
  - The shape of the slope is given by Equation 6. The slope is nonlinear because the maximum rated junction temperature of the LDO is controlled by the power dissipation across the LDO; thus when $V_{IN} – V_{OUT}$ increases the output current must decrease.
- The rated input voltage range governs both the minimum and maximum of $V_{IN} – V_{OUT}$.

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## Application Information (continued)

Figure 30 shows the recommended area of operation for this device on a JEDEC-standard high-K board with a $R_{\theta JA}$ as given in the *Recommended Operating Conditions* table.

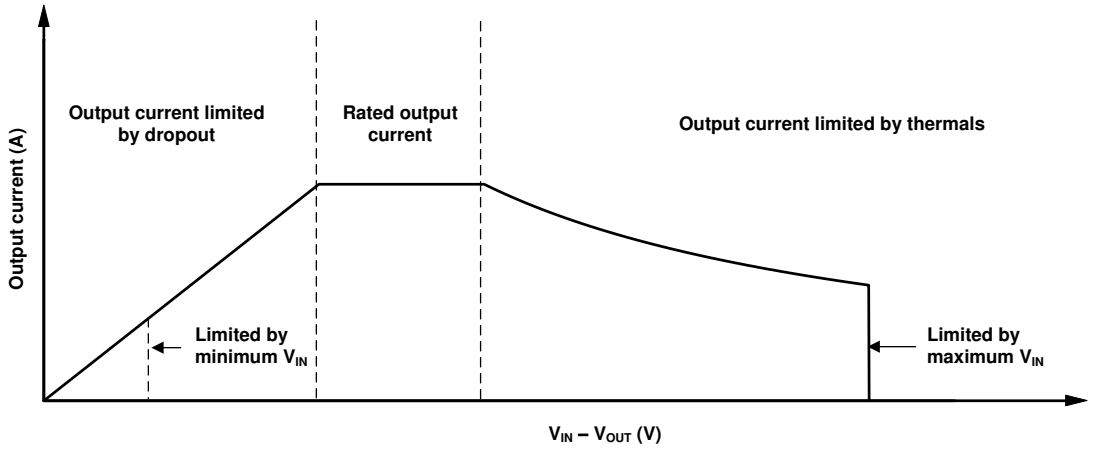



**Figure 30. Region Description of Continuous Operation Regime**

## 8.2 Typical Application

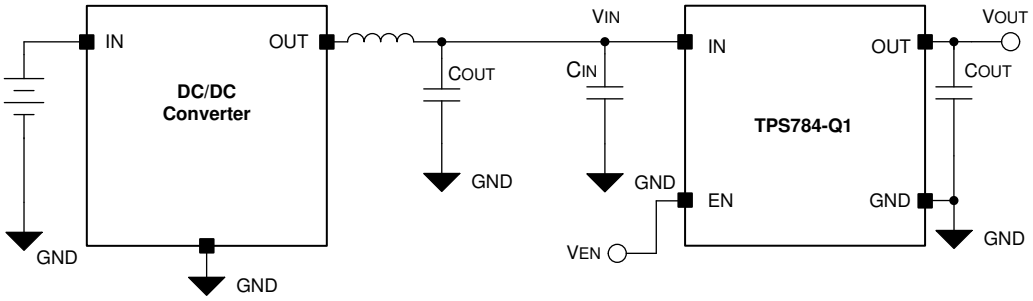



**Figure 31. Operation From a DC/DC Converter**

### 8.2.1 Design Requirements

Table 2 summarizes the design requirement for this application.

**Table 2. Design Parameters**

| PARAMETER | DESIGN REQUIREMENT |
|---|---|
| Input voltage | 3.8 V |
| Output voltage | 3.3 V, ±2% |
| Output load | 300 mA |
| Maximum ambient temperature | 85°C |

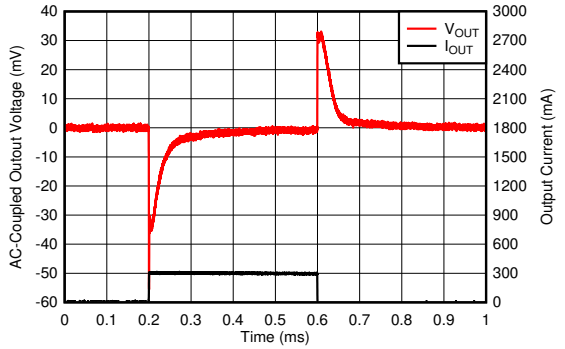
### 8.2.2 Detailed Design Procedure

For this design example, the 3.3-V, fixed-version device is selected. The device is powered of a DC/DC converter connected to a battery. A 500-mV headroom between $V_{IN}$ and $V_{OUT}$ is used to keep the device within the dropout voltage specification and to ensure the device stays in regulation under all load and temperature conditions for this design.

ADVANCE INFORMATION

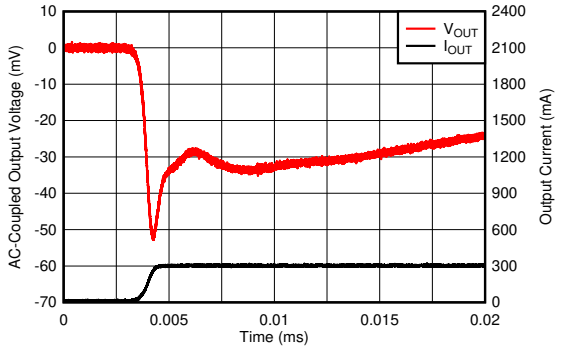
### 8.2.3 Application Curves

Figure 32 through Figure 34 show a zoomed-in captures of load transient behavior for this application.



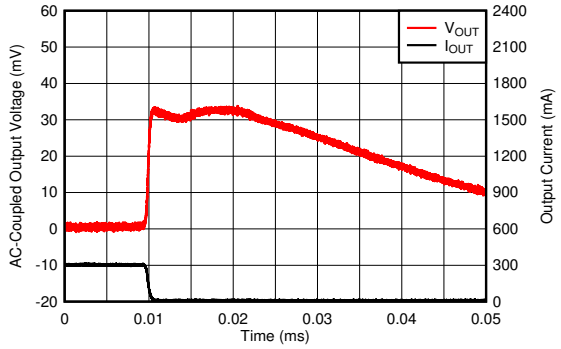

$V_{IN}$ = 3.8 V, $V_{OUT}$ = 3.3 V, $I_{OUT}$ slew rate = 0.5 A/µs

**Figure 32. $I_{OUT}$ Transient From 1 mA to 300 mA**




$V_{IN}$ = 3.8 V, $V_{OUT}$ = 3.3 V, $I_{OUT}$ slew rate = 0.5 A/µs

**Figure 33. $I_{OUT}$ Transient From 1-mA to 300-mA Rising Edge**




$V_{IN}$ = 3.8 V, $V_{OUT}$ = 3.3 V, $I_{OUT}$ slew rate = 0.5 A/µs

**Figure 34. $I_{OUT}$ Transient From 1-mA to 300-mA Falling Edge**

## 9 Power Supply Recommendations

This device is designed to operate from an input supply voltage range of 1.65 V to 6.0 V. The input supply must be well regulated and free of spurious noise. To ensure that the output voltage is well regulated and dynamic performance is optimum, the input supply must be at least $V_{OUT(nom)}$ + 0.5 V. TI requires using a 1-µF or greater input capacitor to reduce the impedance of the input supply, especially during transients.

ADVANCE INFORMATION

# 10 Layout

## 10.1 Layout Guidelines

- Place input and output capacitors as close to the device as possible.
- Use copper planes for device connections, in order to optimize thermal performance.
- Place thermal vias around the device to distribute the heat.
- Only place tented thermal vias directly beneath the thermal pad of the DRB package. An untented via can wick solder or solder paste away from the thermal pad joint during the soldering process, leading to a compromised solder joint on the thermal pad.

### 10.1.1 Additional Layout Considerations

The high impedance of the FB pin makes the regulator sensitive to parasitic capacitances that may couple undesirable signals from nearby components (especially from logic and digital devices, such as microcontrollers and microprocessors); these capacitively-coupled signals may produce undesirable output voltage transients. In these cases, TI recommends using a fixed-voltage version of the device, or isolating the FB node by placing a copper ground plane on the layer directly underneath the LDO circuitry and FB pin to minimize any undesirable signal coupling.

## 10.2 Layout Examples

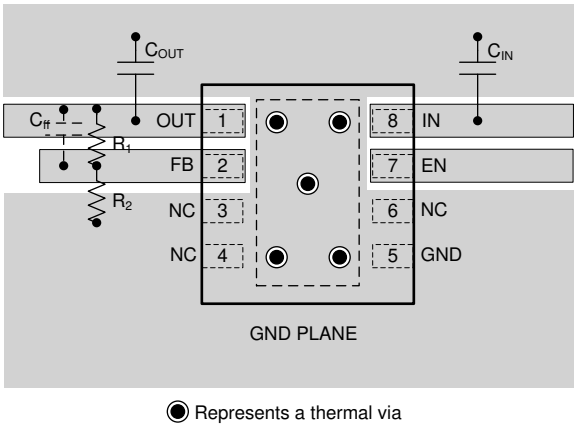



**Figure 35. Layout Example for the DRB Package Adjustable Version**

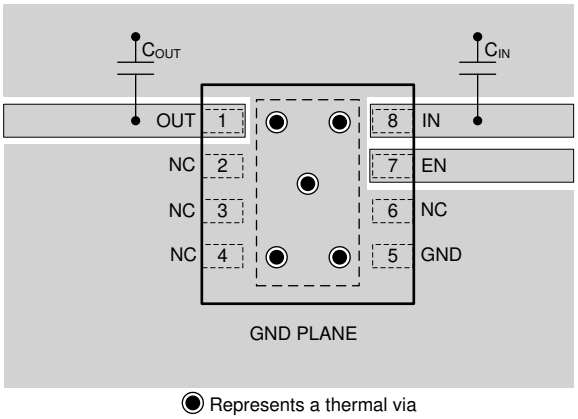



**Figure 36. Layout Example for the DRB Package Fixed Version**

ADVANCE INFORMATION

## Layout Examples (continued)

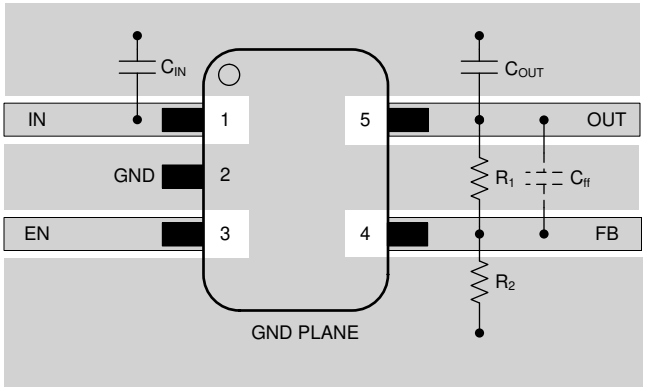



**Figure 37. Layout Example for the DBV Package Adjustable Version**

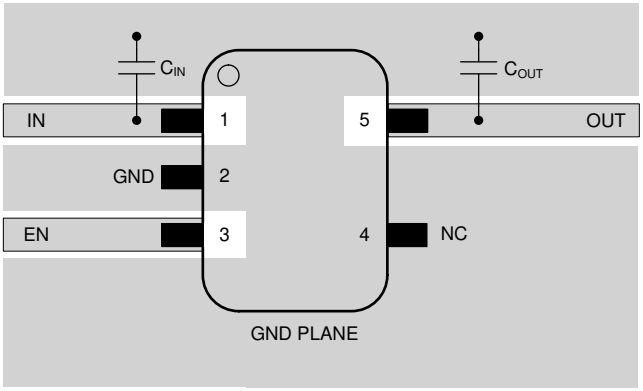



**Figure 38. Layout Example for the DBV Package Fixed Version**

ADVANCE INFORMATION

# 11 Device and Documentation Support

## 11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 11.2 Community Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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## 11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

## 11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PTPS78401QDBVRQ1 | ACTIVE | SOT-23 | DBV | 5 | 3000 | TBD | Call TI | Call TI | -40 to 150 | | Samples |
| PTPS78433QDBVRQ1 | ACTIVE | SOT-23 | DBV | 5 | 3000 | TBD | Call TI | Call TI | -40 to 150 | | Samples |
| PTPS78450QDBVRQ1 | ACTIVE | SOT-23 | DBV | 5 | 3000 | TBD | Call TI | Call TI | -40 to 150 | | Samples |
| TPS78401QDBVRQ1 | PREVIEW | SOT-23 | DBV | 5 | 3000 | TBD | Call TI | Call TI | -40 to 150 | | |
| TPS78433QDBVRQ1 | PREVIEW | SOT-23 | DBV | 5 | 3000 | TBD | Call TI | Call TI | -40 to 150 | | |
| TPS78450QDBVRQ1 | PREVIEW | SOT-23 | DBV | 5 | 3000 | TBD | Call TI | Call TI | -40 to 150 | | |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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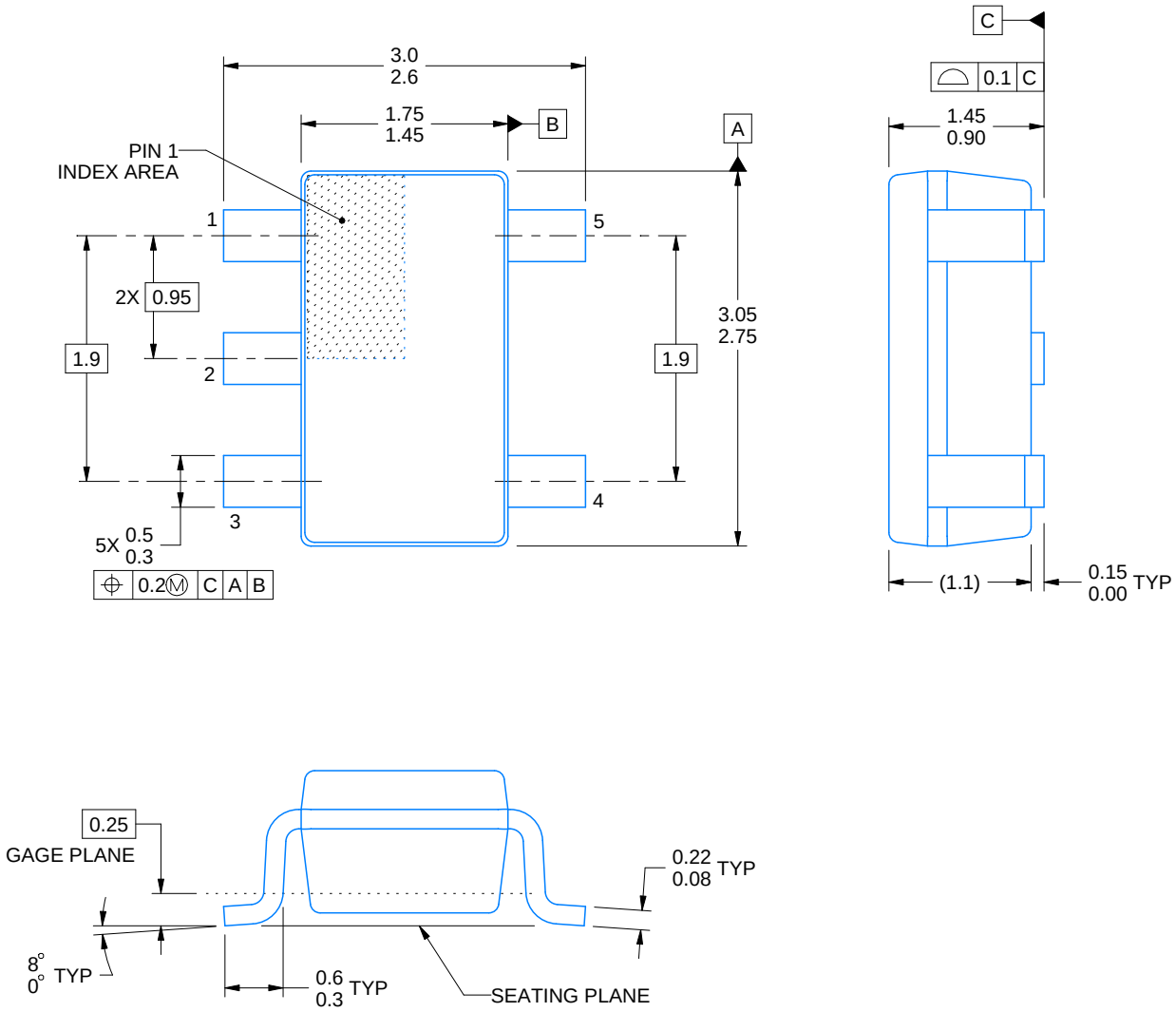
# PACKAGE OUTLINE

## DBV0005A

## SOT-23 - 1.45 mm max height

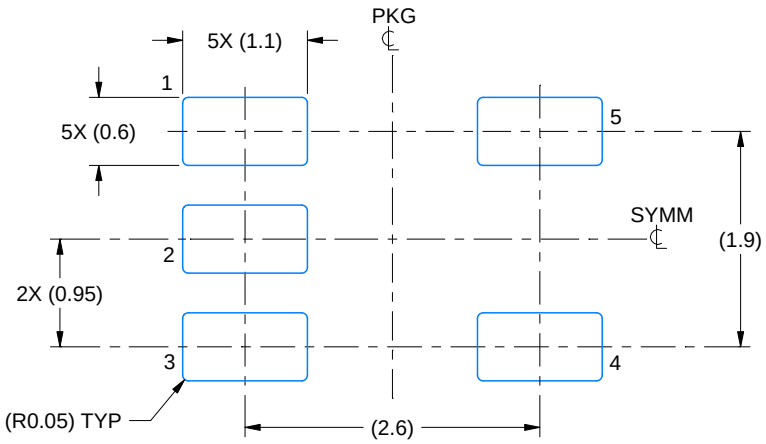
SMALL OUTLINE TRANSISTOR



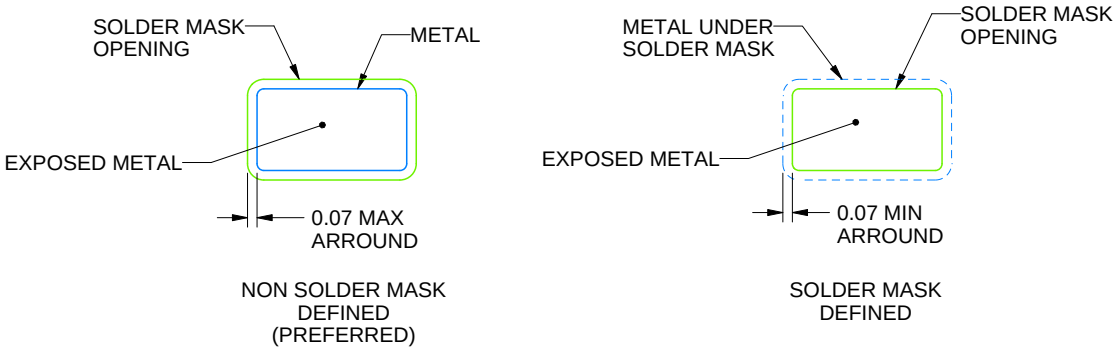

4214839/E 09/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

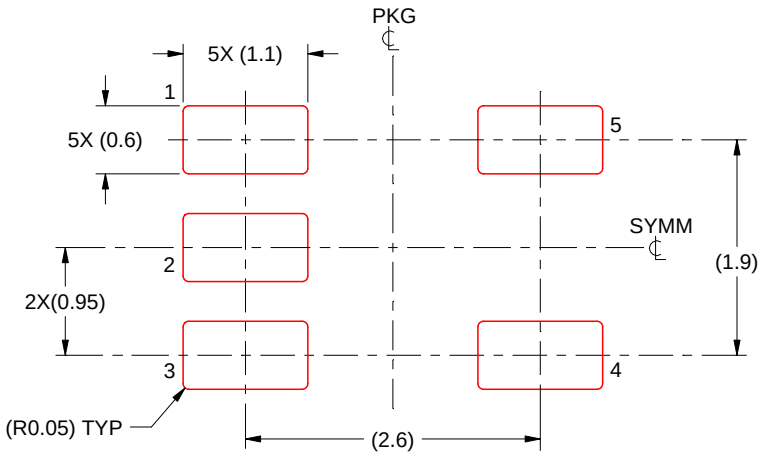



SOLDER MASK DETAILS

4214839/E 09/2019

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/E 09/2019

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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